Comparison of Various Systems On Chip Buses - A Case Study

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Abstract—*There are number of embedded buses available for designing of Microcontrollers. These buses are defines a system on-chip communication standard for designing high-performance embedded Microcontrollers.There are several buses available like wishbone bus, core connect bus, and Avalon bus. These buses are from different-different owners with their own well- defined standards and specifications. These buses are different in the way like the data bus width, address bus width, architecture, timing, operating frequency. The purpose of this paper is to choose a SoC bus for Open Cores that we would adopt and use in any core development. Standardizing on a common SoC will help us as a community to produce cores that can be easily integrated together to design Microcontroller.*

I. INTRODUCTION

This paper described overview and comparison between embedded buses which defines a system on-chip communication standard for designing high-performance embedded microcontrollers. Functions of the all buses are same: connecting IP cores, they all provide basic handshaking and variable data bus sizes. . Basic idea is to perform the proper and lossless communication between the IP cores which uses same protocols on the System on Chip (SOC) system. Basically, a SOC is a system which is considered as a set of components and interconnects among them.

The flow of data will happen in the system in order to achieve a successful process to complete for which the various interfaces are required. If these interfaces have issues, then the process to be achieved will fail which leads to affects the whole application. Generally, what happen in an SOC system, the protocols can be used as interfaces which will be based on the application and also the designer. The interface has its own properties which suits for the corresponding application. This paper work is chosen because currently the issues are increased in the industries due to the lack of proper data transferring between the IP cores on the System on Chip (SOC) system. Hence to resolve this issue or to solve this problem, the standard protocol buses are used in order to interface the two IP cores. Here the loss of data depends on the standards of protocols used.

Most of the IP cores from ARM use AMBA (Advanced Microcontroller Bus Architecture) which has AHB (Advanced High-Performance Bus), ASB (Advanced System Bus), and APB (Advanced Peripheral Bus). This bus has its own advantages, disadvantages and flexibilities. AVALON is Altera's interface bus used by the Nios embedded processor. The AVALON switch fabric has a set of pre-defined signal types with which a user can connect one or more intellectual property (IP) blocks. CORECONNECT is an IBM-developed on-chip bus communications link The WISHBONE System-on-Chip (SOC) Interconnect Architecture for Portable IP Cores from Silicore Corporation. Above discussion shows the basic description and requirements for the System-on-chip (SOC). And buses are introduced which are useful to perform lossless and proper communication between the IP cores.

II. OVERVIEW OF ALL BUSES

A. AMBA BUS

The Advanced Microcontroller Bus Architecture (AMBA) specification [2] defines an on chip communications standard for designing high-performance embedded Microcontrollers. Three distinct buses are defined within the AMBA specification:

- Advanced High-performance Bus (AHB)
  The AMBA AHB is for high-performance, high-clock-frequency system modules. The AHB acts as the high-performance system backbone bus.
- Advanced System Bus (ASB)
  The AMBA ASB is for high-performance system modules. It is an alternative system bus suitable for use where the high- performance features of AHB are not required.
- Advaced Peripheral Bus (APB)
  AMBA APB is optimized for minimal power consumption and reduced interface complexity to support peripheral functions. APB can be used in conjunction with either version of the system bus Depending on the requirements.

If we refe the new specification of the AMBA that is AMBA 3 and AMBA 4 that defines five distinct buses. Three buses are same as AMBA specification 2 and in that two new buses are added.

- Advanced Extensible Interface (AXI)
  The third generation of AMBA interface defined in the AMBA 3 specification, is targeted at high performance, high clock frequency system designs and includes features which make it very suitable for high speed sub-micrometer interconnect.
- Advanced Trace Bus (ATB)
  The Advanced Trace Bus (ATB) is used as part of the Core Sight on-chip debug and trace solution.

The objective of the AMBA specification is to:

- Facilitate right-first-time development of embedded microcontroller products with one or more CPUs, GPUs or signal processors,Be technology independent, to allow reuse of IP cores, peripheral and system macro cells across diverse IC processes.
- Encourage modular system design to improve processor independence, and the development of reusable

peripheral and system IP libraries
- Minimize silicon infrastructure while supporting high performance and low power on-chip communication

Designer has to choose which busses he will use or when to use right bus. The choice between AHB and ASB will not be easy, as they try to address the same type of devices. It will be a difficult choice when you keep in mind that there's no clear path integrating Devices between ASB and AHB.

The Figure 1 shows the typical AMBA system which consist of all three buses. An AMBA-based Microcontroller typically consists of a high-performance system backbone bus (AMBA AHB or AMBA ASB), able to sustain the external memory bandwidth, on which the CPU, on-chip memory and other Direct Memory Access (DMA) devices reside. This bus provides a high-bandwidth interface between the elements that are involved in the majority of transfers. Also located on the high performance bus is a bridge to the lower bandwidth APB, where most of the peripheral devices in the system are located. APB is mostly useful for connection to the lower power devices like keypad, LCD display, and timer.

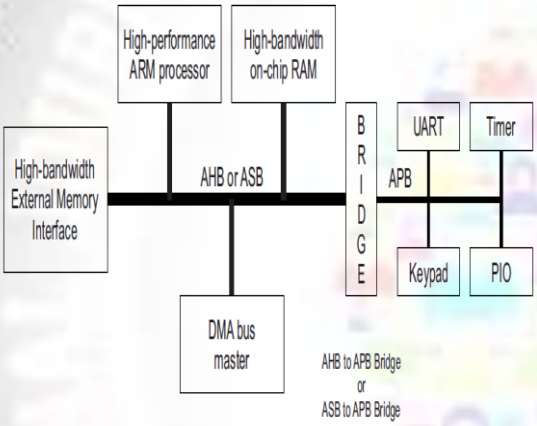

Fig. 1: A typical AMBA system [2]

The AMBA AHB and AMBA ASB are designed to be used with a central multiplexor interconnection scheme. They both have multi master multi slave capabilities. They can support up to 16 masters and 16 slaves to gather. The arbitration process used by arbiter to choose which master is active. In this only one master is active at one time no other master is allowed to access the bus at the same time. A central decoder is also required to control the read data and response signal multiplexor, which selects the appropriate signals from the slave that is involved in the transfer.

B. WISHBONE BUS

The WISHBONE System-on-Chip (SOC) Interconnect Architecture [3] for Portable IP Cores from Silicore Corporation. It is a portable interface for use with semiconductor IP cores. Its purpose is to foster design reuse by alleviating system on- a-chip integration problems. This is accomplished by creating a common, logical interface between IP cores. The WISHBONE interconnect is intended as a general purpose interface. As such, it defines the standard data exchange between IP core modules. This can improve the portability and reliability of the system, and results in faster time-to-market for the end user. And we can compare the WISHBONE bus with the Microcomputer bus that provides a flexible integration solution and also offer a variety of bus cycles and data path widths to solve various system problems The Figure 2 shows the basic implementation of the wishbone bus. WISHBONE uses master/slave architecture. That means that functional modules with master interfaces initiate data transactions to participating slave interfaces. As shown in Figure below, the masters and slaves communicate with each other through an interconnection interface called the INTERCON. The INTERCON is best thought of as a 'cloud' that contains circuits. These circuits allow Masters to communicate with Slaves. The cloud analogy is used because WISHBONE can be modelled in a similar way. Master and Slave interfaces communicate thorough an interconnection.

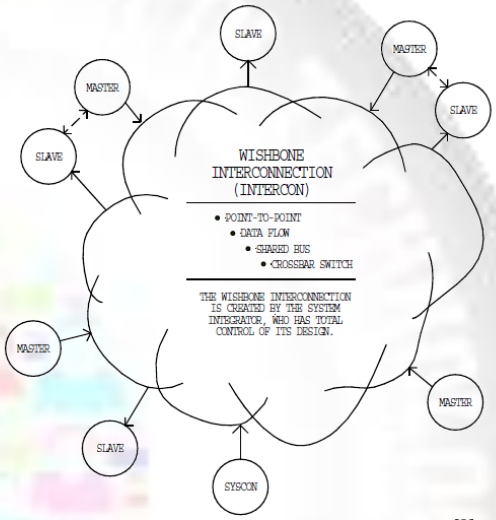

Fig. 2: Implementation of wishbone bus [3]

The Wishbone specification is different from other specifications, as it makes use of RULES, RECOMMENDATIONS, SUGGESTIONS, PERMISSIONS and OBSERVATIONS. This allows Wishbone to be a simple, open, highly configurable interface.

The Figure 3 show the off-chip interconnection of WISHBONE bus. An off-chip interconnection is used when a WISHBONE interface extends off-chip.

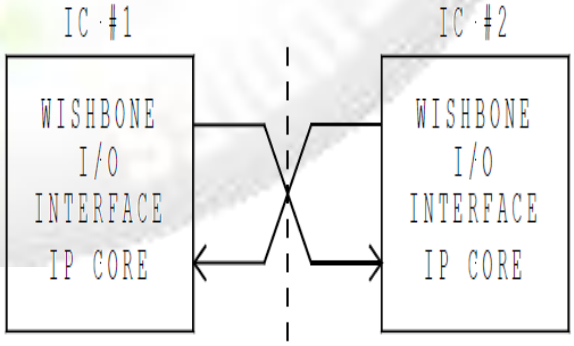

Fig. 3:Off-chip interconnection [3]

An interconnection system that supports a single WISHBONE master and a single WISHBONE slave interface is known as point to point connection. It is the simplest way to connect two cores. The figure of point to point interconnection is same as off chip interconnection

with the difference one acting as a master and other as a slave.

The data flow interconnection is as shown in the Figure 4. It is used when data is processed in a sequential manner.

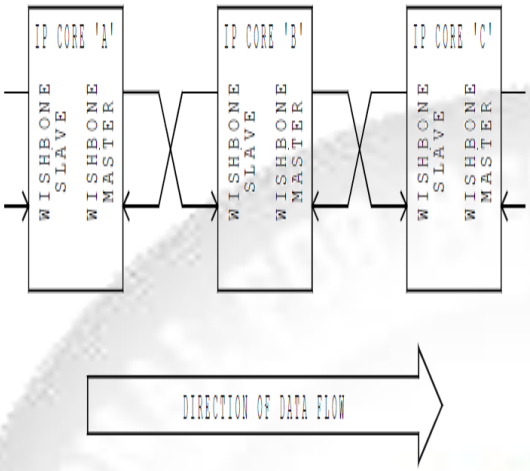

Fig. 4:Data flow interconnection [3]

The crossbar switch interconnection is used when connecting two or more WISHBONE Masters together so that each can access two or more Slaves. The Figure 5 shows the crossbar interconnection.In the crossbar interconnection, a Master initiates an addressable bus cycle to a target Slave. An arbiter determines when each Master may gain access to the indicated Slave.

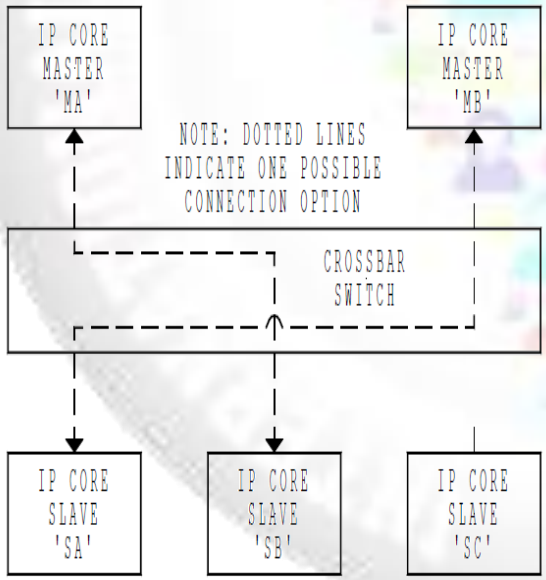

Fig. 5: Crossbar (switch) interconnection [3]

C. AVALON BUS

Avalon is Altera's interface bus used by the Nios embedded processor The Avalon bus is a simple bus architecture designed for connecting on-chip processors and peripherals together into a system–on–a–programmable chip (SOPC). The Avalon bus is an interface that specifies [4] the port connections between master and slave components, and specifies the timing by which these components communicate. The Avalon switch fabric has a set of pre-defined signal types with which a user can connect one or more intellectual property (IP) blocks.

The Avalon bus supports multiple bus masters. This multi-master architecture provides great flexibility in the construction of SOPC systems, and is amenable to high bandwidth peripherals. The advanced transfers include streaming transfers, read transfers with latency and bus control signals. Avalon masters and slaves interact with each other based on a technique called slave-side arbitration. Slave-side arbitration determines which master gains access to a slave, in the event that multiple masters attempt to access the same slave at the same time.

The Figure 6 shows the basic bus module of AVALON bus The AVALON bus module (an AVALON bus) is a unit of active logic that takes the place of passive, metal bus lines on a physical PCB. Ports of the Avalon bus module could be thought of as the pin connections for all peripheral devices connected to a passive bus. AVALON bus specify following services.

- Data-Path Multiplexing
- Address Decoding
- Wait-State Generation
- Interrupt-Priority Assignment
- Streaming Read and Write Capabilities
- Dynamic Bus Sizing

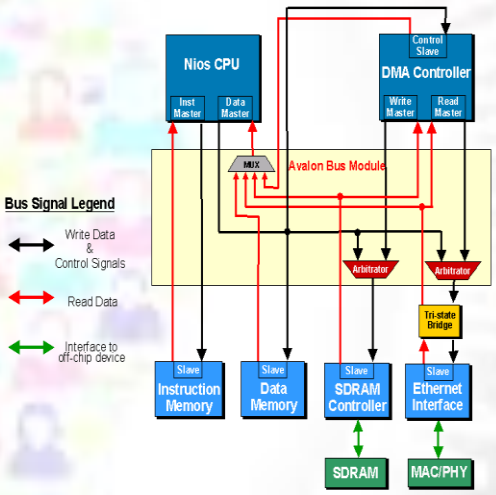

Fig. 6: Avalon Bus Module Block Diagram [4]

D. CORE CONNECT BUS

The IBM Blue Logic cores program provides the framework to efficiently realize complex system-on-chip (SOC) designs. The Core Connect technology [6] eases the integration and reuse of processor, system, and peripheral cores within standard product platform designs to achieve overall many single chip solutions used in applications today are designed as custom chips, each defines by its own internal architecture. Logical units within such a chip are often difficult to extract and re-use in different applications. As a result, we can say that many times the same function is redesigned from one application to another. Promoting reuse by ensuring that the macro interconnectivity is accomplished by using common buses for communications.

The IBM Core Connect architecture provides three buses for interconnecting cores, library macros, and custom logic:

- Processor Local Bus (PLB)
  The PLB bus addresses the high performance, low latency system modules and provides the design

flexibility needed in a highly integrated SOC.

- On-Chip Peripheral Bus (OPB)
  The OPB bus is optimized to connect to lower speed peripherals and low power consumption.
- Device Control Register (DCR) Bus

The Device Control Register (DCR) bus is designed to transfer data between the CPU's general purpose registers (GPRs) and the DCR slave logic's device control registers (DCRs). The DCR bus removes configuration registers from the memory address map, which reduces loading and improves bandwidth of the PLB. The fully synchronous DCR bus provides 10-bit address bus and 32-bit data bus. The DCR bus is typically implemented as a distributed mux across the chip. Below diagram illustrates the structure of Core Connect bus. Core Connect defines a clear structure for all system components and how they connect. The daisy-chained DCR bus provides a relatively low-speed data path for passing configuration and status information. The DRC bus wraps in daisy chain configuration through all components attached to the PLB. In this figure high performance CPU core high performance memory resides on PLB. While the OPB hosts lower data rate peripherals like keyboard, timer LCD display as shown in Figure 7.

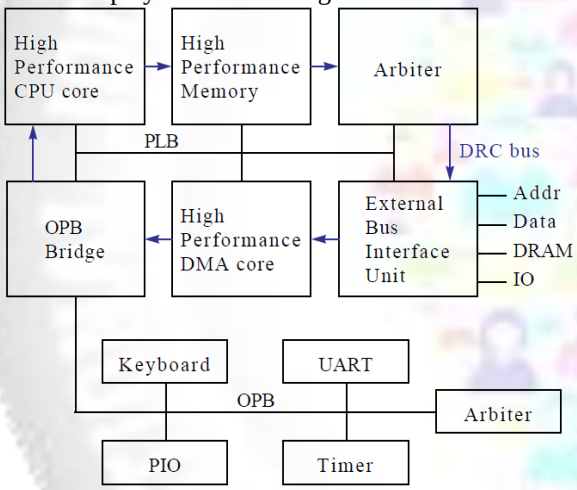

Fig. 7:Logical Core connect Bus Structure [6]

III. COMPARISON

These buses are from different owners as mentioned in above section. These buses are different in terms of data width, address width, frequency and its architecture. Operating frequency of the AMBA ,WISHBONE and AVALON bus are user defined and maximum frequency of core connect bus is 183 MHz If we compare the buses in terms of data bus width the AMBA AHB bus has wider data bus width as compare to all other buses AMBA AHB can support up to 1024 bits of data bus width. AMBA ASB support up to 256 bits of data bus width. AMBA APB which support up to 32 bits of data bus width .WISHBONE bus can support 8 to 64 bits of data bus width. AVALON bus can support 8, 16 and 32 bits of data bus width. In CORECONNECT the PLB can support up to 256 bits of data bus width. OPB and DCR can support up to 32 bits of data bus width. If we compare the architecture of all buses. The AMBA AHB and ASB is (Multi) master (max 16) / (Multi) slave type of architecture. AMBA APB is (Single) Master (bridge) / (Multi) Slave type of architecture. And all other buses like WISHBONE, AVALON and CORECONNECT are (Multi) Master / (Multi) Slave type of architecture. Address bus width of AMBA, AVALON and CORECONNECT (PLB and OPB) are 32bit.coreconnect DCR is only 10 bit address bus width. As compare to all bus if we require the more width then the WISHBONE bus can be used which has 8 to 64 bit address width. If we compare in terms of design technology all buses are technology independent except the AVALON bus which can be implemented on Altera devices using SOPC. If we compare the timing specification all buses has Synchronous, well defined timing specification. Interconnection wise also all buses are different in nature. AMBA AHB has multiplexed implementation. Interconnection of AMBA ASB and APB is not defined. There are four types of interconnection like point to point Data flow, shared bus Crossbar switch specified by the WISHBONE bus which explained above. In CORECONNECT bus specified multiplexed implementation.

IV. CONCLUSION

Finally I can conclude that all embedded buses are useful for the defining a system on-chip communication standard for designing high-performance embedded microcontrollers. If we want more data bus width then we can use AMBA AHB bus. If we require wider Address bus width we can use the WISHBONE bus which has wider address bus width. If someone wants to connect more devices then they can use AMBA bus which can support up to 16 Master and 16 Slave the benefits of the SOC approaches are numerous, including improvements in system performance, cost, size, power dissipation, and design turn-around time. All buses are useful for the different applications as all have different-different parameter as mentioned above. All buses are useful to perform the proper and lossless communication between the IP cores which using same protocols on the System on Chip (SOC) system.

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