Design of High-Speed Comparator for LVDS Receiver

[1]Jayesh S. Shetti Karwarker [2]Dr. H. G. Virani
[1]PG Scholar [2] Associate Professor
[1, 2]Electronics & Telecommunication DepartmentGoa College of Engineering Farmagudi, Ponda, Goa

Abstract—*Ever increasing demands of the processing speeds require very high speed and power efficient interconnections between the ICs. Such connections are governed by various standards, LVDS is one among them. In order to meet the requirements of high speed, low noise communication between ICs, the Low Voltage Differential signalling (LVDS) protocol is used. This paper studies the design of comparator stage of LVDS receiver. Due to the differential transmission technique and the low voltage swing, LVDS allows high transmission speeds and low power consumption at the same time. The proposed circuitry has been simulated properly in 180 nm CMOS process technology using Cadence Spectre simulator.*

Keywords: *CMOS, LVDS, Comparator.*

I. Introduction

Board level chip interfaces are demanding very high speed, power efficient interfaces. The ever increasing processing speed of microprocessor motherboards, optical transmission links, intelligent hubs and routers, etc..., pushing the off-chip data rate into the gigabits-per second range. However, unlike internal clocks, chip-to-board signaling gains little benefit in terms of operating frequency from the increased silicon integration. In the last decade, high data rates were achieved by massive parallelism, with the disadvantages of increased complexity and cost for the IC package and the printed circuit board (PCB). For this reason, the off-chip data rate is expected to move to the range of Gb/s-per-pin in the near future. [2] [3]

While the reduction of the power consumption is of great concern in battery-powered portable systems, it is also required in other systems to reduce the costs related to packaging and additional cooling systems. Some of today's biggest challenges that remain to be solved include the ability to transfer data at fastest rate possible, low power systems than currently available and economical solutions to overcome the physical layer bottleneck.

Data transmission standards like RS-422, RS-485, SCSI and others have their own limitations notably in transferring raw data across a medium. Optical fibers are also costly and area inefficient for long distances. Thus, low-cost, high-speed parallel links and serial links using copper cables are an attractive solution for such applications. In this regard, Low-voltage Differential Signaling (LVDS) technology was developed in order to provide a low-power and low-voltage alternative, to other high-speed I/O interfaces for point-to point transmission.[4][5]

Current mode operations have been considered as an alternative in analog circuit designs as CMOS VLSI devices are scaled down in size. Comparators are used in data converters and other front end signal processing applications. Voltage comparator encounters several difficulties including operational frequency, input offset voltage and power consumption. Current comparison has been done by impressing the current pulse signal at the input of the comparator and finding whether it is positive or negative. The output voltage generated by the comparator is used properly to indicate the result of operation. Circuit uses source follower input stage and a CMOS inverter as a positive feedback.

II. Comparator Design

Comparator blocks are designed to meet the defined specifications of LVDS receiver compliant to IEEE 1596.6 at 1GHz. Comparator first amplifies this differential input with a certain high gain around 6-10 using NMOS differential amplifier. Such a double ended output of NMOS differential amplifier is converted to single ended full rail output of 0-3.3V by source follower.

Comparator consists of two stages as NMOS differential amplifier and source follower. M5 is made to sink a constant current hence M5 should be kept in saturation. Common mode of input should be such that M1 and M2 are in saturation. The gain of NMOS differential amplifier is around 6-10.When the current through M1 is more than that of M2, VA is less than Vb. Similarly when the current through M2 is more than that through M1, VA is more than Vb.

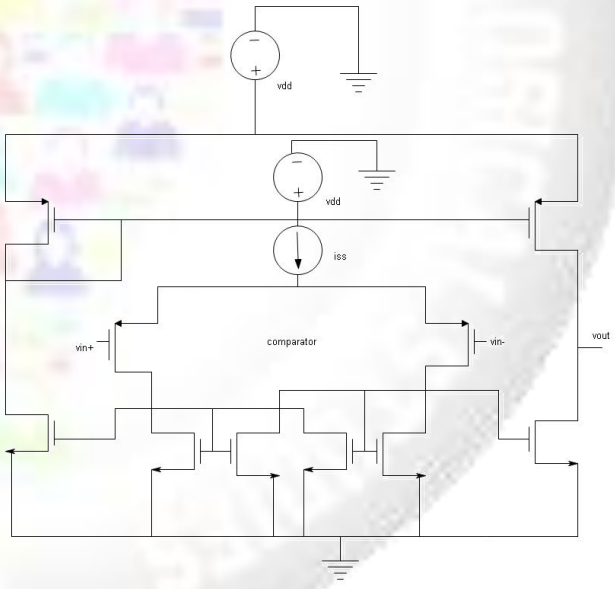

Fig.1: Comparator Circuit Diagram

Electrical specifications for comparator

All the specifications of the system are derived in accordance with the IEEE 1596.3 - 1996 Std. [1]

Input common mode voltage =1.65 V

Input differential voltage=+300m V to -300m V

Output single ended voltage=3.3V

Dv =3.3V

DT=10% of frequency of operation

= 10% (1ns) =0.1nS

SR=dv/dt =3.3/0.1*10^{-9} =33V/nS

SR=ID/CL

ID=SR*CL=33*10^{9}*10 *10^{-6}

=330µA

µPC_{OX}=55

µnC_{O4X} = 293

V DS=0.3V

VDS=V GS-VT

0.3> VGS-0.5

0.8 > VGS

VGS < 0.8

So, V_{G4S} = 0.7

V_T =0.5V

I_T=µnC_{OX} (W_6/L_6)n (V_{GS}-V_T)^2

(W_6/L_6)$_p$ = IT/ μ_{nOX} (V_{GS}-V_T)^2

=330*10^{-6}/55*10^{-6}*$(0.2)^2$ = 150 µm

For better operation

(W_6/L_6)$_p$=100 µm

Current divides at pm3 and pm4

(W_0/L_0)$_p$=50 µm

(W_3/L_3)$_p$=50 µm

Again same current flows at pm2 and pm1

(W_2/L_2)$_p$=100 µm

(W_1/L_1)$_p$=100 µm

Inverter design

Same current flows through inverter

(W_{12}/L_{12})$_p$=100 µm

(W_{14}/L_{14})$_p$=100 µm

(W_{18}/L_{18})$_n$=20 µm

(W_{20}/L_{20})$_n$=20 µm

III. Simulation Results

The schematic design and layout design are carried out using CADENCE tool for 0.18µm technology (UMC180nm).

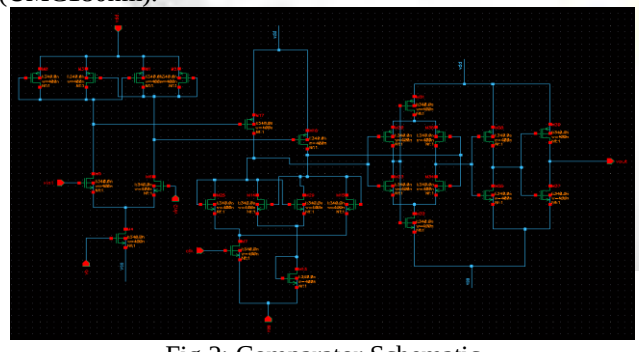

Fig.2: Comparator Schematic

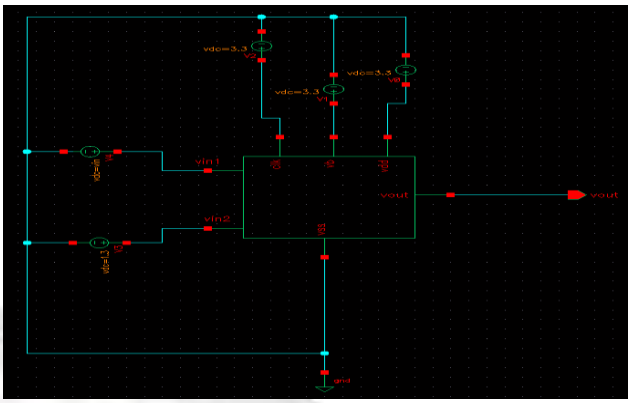

Fig.3: Comparator DC Schematic

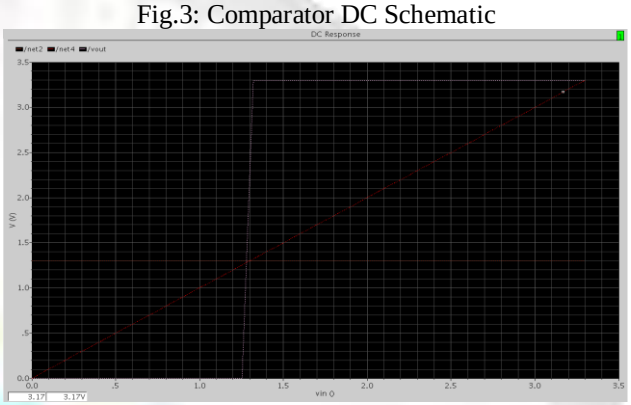

Fig.4: Comparator DC Response

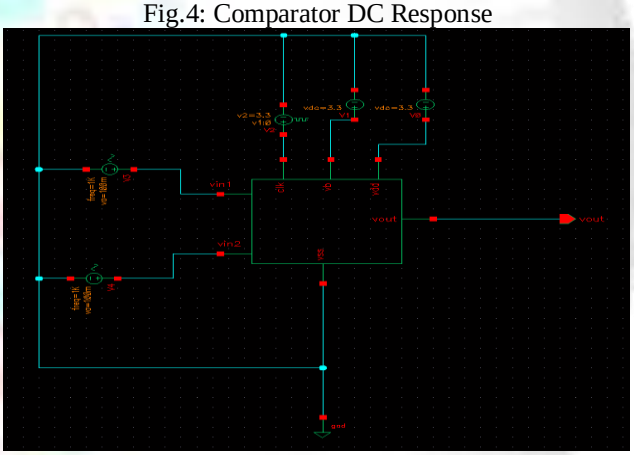

Fig. 5: Comparator AC Schematic

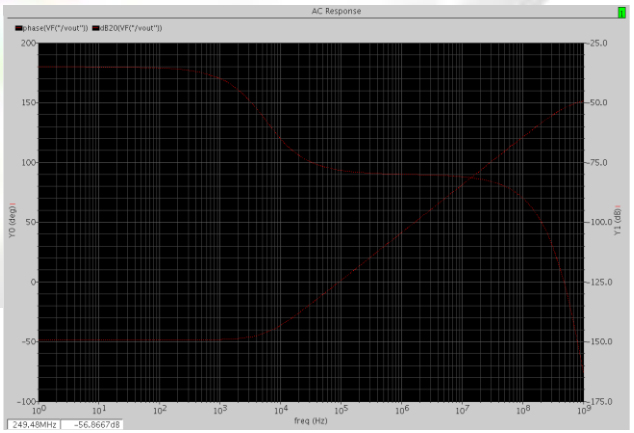

Fig.6: Comparator AC Response

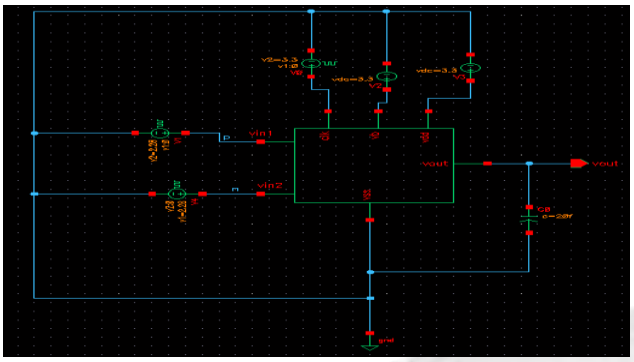

Fig.7: Comparator Transient Schematic

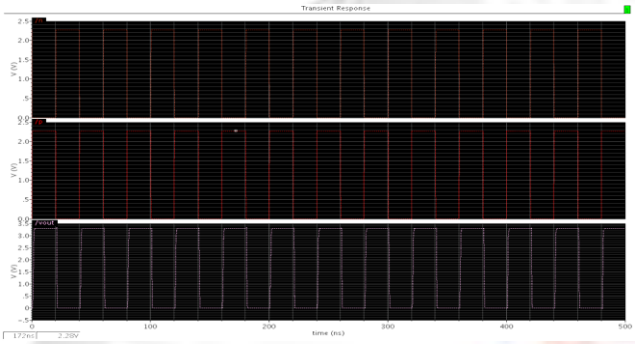

Fig.8: Comparator Transient Response

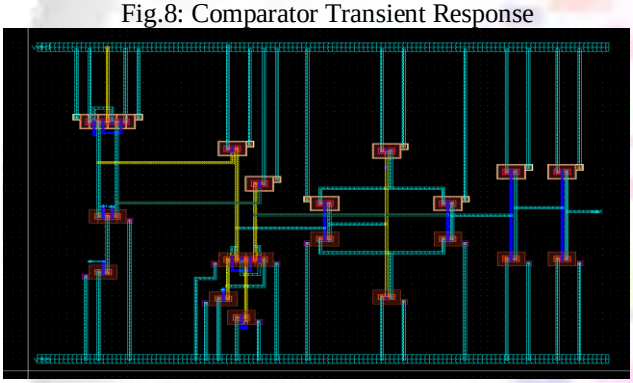

Fig.9: Comparator Layout

IV. CONCLUSION

High-Speed Comparator for LVDS Receiver was designed at 0.18um technology.

REFERENCES

[1] IEEE standard for low-voltage differential signals (lvds) for scalable coherent interface (sci), 1596.3 sci-lvds standard. IEEE Std.1596.3-1996, 1994.

[2] Sung-Jun Song Sung-Sik Song Wang-Joo Lee Hoi-Jun Yo0 Jaeseo Lee, Jae-Won Lim. Design and implementation of cmos lvds 2.5gb/s transmitter and 1.3gb/s receiver for optical interconnections, 2008.

[3] Wei Feng Hao Cui Lingyi Huang Weiwu Hu Feng Zhang, Zongren Yang. A high speed cmos transmitter and rail-to-rail receiver. 4TH IEEE international symposium of electronics design, test and applications, 2008.

[4] Davide Vecchi Andrea Boni, Andrea Pierazzi. Lvds i/o interface for gb/s-per-pin operation in .35m cmos. IEEE J. Solid-state circuits, 36:706–711, April 2001.

[5] B.Young. A soi cmos lvds driver and receiver pair. IEEE Symposium on VLSI Circuits, pages 153–154, 2001.

[6] Razavi. B. Design of Analog CMOS Integrated Circuits. McGraw Hill,2001, NewYork.

[7] B.Young. A soi cmos lvds driver and receiver pair. IEEE Symposium on VLSI Circuits, 2001.

[8] Tai-Ping Sun Chung-Yuan Chen, Jia-HongWang. A novel mini-lvds receiver in 0.35- um cmos, 2001.

[9] Alan Hasting. The art of analog layout. Prentice Hall, 1, 2000.

[10] Douglas R Holberg Philip E Allen. CMOS Analog Circuit Design. Oxford University press, New York.