# A 1-V, 10-Bit, 40MS/S CMOS Pipelined Analog to Digital Converter

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**Abstract**—*Analog-to-digital converters (ADCs) are required in almost all communication and signal processing applications. This paper describes a 1-v, 10-bit, 40-Msample/s pipeline Analog-to Digital converter in 45nm CMOS technology. The entire circuit architecture is built with a modular approach consisting of identical units organized into an easily expandable pipeline chain. The ADC consumes a 1.14mw at a sampling rate of 40MS/s. Comparator is designed using latch type voltage sense amplifier. The ADC will help to reduce the power consumption of system-on-a-chips (SOCs) for digital consumer products and wireless communication equipment.*
**Keywords: -** Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), Sample and Hold circuit, Comparator, system-on-a-chips (SOCs), Operational Amplifier.

## I. INTRODUCTION

The continuous effort to improve the performance of analog-to-digital converters (ADC) has led the development of several precision techniques for ADC's. The primary objective of those precision techniques is to alleviate the accuracy constraints such as capacitor mismatch, charge injection, finite op amp DC gain and comparator offset.

ADCs are rarely used alone, but are often included in more elaborate systems. The performance of the ADCs will affect the performance of the system where it is included and the precision with which the ADC parameters are known is necessary to compute the precision of the final result of the system using it. The rapid growth of the signal processing applications is driving the pipelined ADC design towards higher speed, higher precision, lower power consumption, lower supply voltage, smaller size and higher levels of integration along with the advancement of the fabrication technology. While continual speed improvement can still be achieved by using the advanced sub-micron or deep sub-micron CMOS processes, data converter designers find it more and more difficult to improve or even keep the accuracy of pipeline ADCs which reply on high gain operational-amplifier (OPAMP) and well matched components to produce high-precision converters. The continuing trend of submicron CMOS technology scaling, which is coupled with lower power supply voltages, makes it possible to keep up with the application development. At low power supply voltage, large open-loop OPAMP gain is difficult to realize without sacrificing bandwidth and/or power consumption [1]. As a result, the finite OPAMP gain is becoming a major hurdle in achieving both high speed and high accuracy in following ways.

First, large open loop OPAMP gain is difficult to realize without sacrificing bandwidth given the continuing trend of submicron CMOS scaling which is coupled with lower power supply voltages. Second, there are some physical limits on the component matching due to process variation, so it cannot be improved continually with CMOS technology scaling [9].

### A. Paper Organization

Section 1 discussed about the Introduction to the ADC. Section 2 discussed about architecture of pipelined ADC and 1.5-bit/stage Pipelined ADC. Section 3 discusses the design of sampling and hold circuit. Section 4 discusses about sub-ADC and the output of it. Section 5 discusses about the sub-DAC and the results of it. Section 6 discusses about the double tail latch type comparator architecture Section 7 discusses about the digital correction logic. Section 8 discussed about the simulation results of 10-bit pipeline architecture. Section 9 details the conclusion of our paper. Section 10 presents the papers and materials referred for implementation of this design.

## II. ARCHITECTURE OF PIPELINED ADC

The PIPELINED Analog-to-Digital converter ADC) has been widely adopted as an optimal architecture for medium-to-high resolution applications. To meet application-specific requirements, research on the pipelined ADC has been mainly driven for the design of a high-speed, low-power, and high-gain Operational amplifier (op-amp) [2]. As CMOS technology scales down, the design of a robust high-gain op-amp is becoming extremely difficult due to the low intrinsic device gain and reduced headroom. Traditional approaches of cascaded amplifiers even fail to generate a sufficient gain in a scaled CMOS, while they still require large power and complicated frequency compensation techniques.

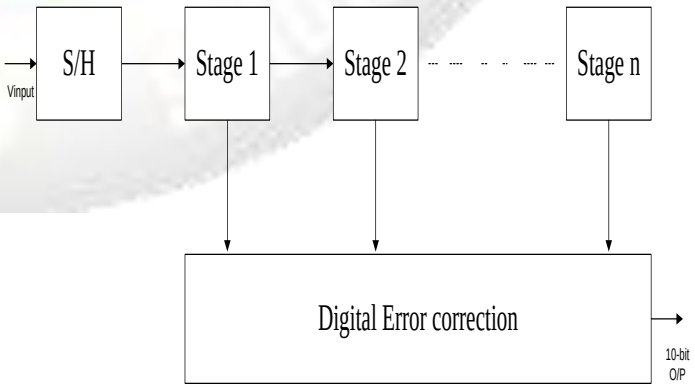


Fig. 1: General Pipeline Architecture

The 10-bit pipelined ADC structure is implemented using 1.5bit/stage architecture.

### *A. Bits/Stage Architecture*

Using 1.5 bits/stage relaxes the requirements on the sub-ADC, so efficient high speed designs can be developed. The 1.5 bits/stage can only have three valid quantization intervals, '00', '01'and '10'. In order to prevent overflow in the digital correction, '11' is not a valid output unless from the last stage [5]. To get M -bits of resolution, M – 1 stageis needed. Using this unique topology, the gain factor can be set to a constant of 2 between stages.

Figure 2 shows a typical structure for a single stage of the 1.5 bits/stage topology. Assuming the input has a range |X | ≤ VR, the quantization interval size is VR /2. The sub-ADC should have thresholds of VR /4 and –VR/4. In practice, the actual ADC thresholds will be different from these 'nominal' values. The digital word is sent to the digital correction portion of the ADC to be combined with all the other stage outputs. The digital output word provides the input to the sub-DAC [3]. This sub-DAC is designed to produce one of three possible output voltages. For the 1.5 bits/stage architecture these voltages are set to VR /2, 0, and –VR /2 for sub-ADC outputs codes 00, 01 and 10 respectively. The sub-DAC output is subtracted from the input and the residual is multiplied by a gain of 2[16]. If the sub-DAC outputs are accurate, this gain will scale the residual error to ±VR (provided the sub-ADC quantization thresholds are within VR /4 of their nominal values). The following stage will then quantize the residual error from this stage.

Digital correction for a 1.5 bits/stage pipeline is fairly simple. Conceptually, the first stage in a pipeline provides the MSB for the final output and as the sample moves through the pipeline, each stage output become less significant and the last stage provides the LSB.

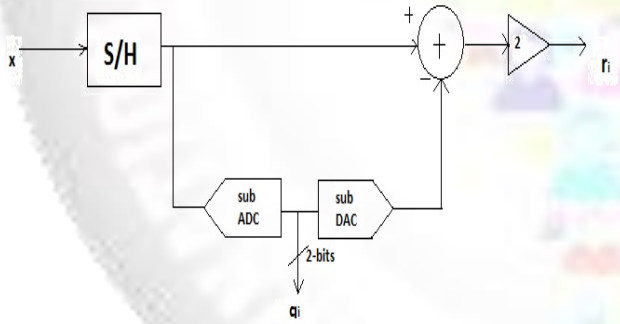


Fig. 2: 1.5-bit/stage architecture

## III. Sampling And Hold

Traditionally, the sample-and-hold circuit in pipelined ADC tends to consist of a sampling network and a sample and-hold amplifier (SHA). The SHA is used to present a held signal to the first pipeline stage. It, however, consumes a significant amount of power, and contributes substantially to the distortion and noise of the whole ADC. This is mainly because it is a front-end block that has to handle the full-swing input signal (and hence the impact on distortion) without any previous amplification (and hence the impact on noise). To overcome these disadvantages, "SHA-less" architecture, in which the sample-and-hold (s/h) circuit is integrated in the first MDAC [7], without a dedicated amplifier. This architecture, provides the same s/h operation but saves power, improves distortion and reduces noise. The first issue of the SHA-less architecture is the need to match the input networks of the flash (sub-adc) and the MDAC of the first stage. Since the flash and the MDAC see the actual input signal, and not a held signal, any mismatch between the bandwidths and/or the sampling instant of these two input networks will result in a mismatch between the sampled values of the MDAC [8].

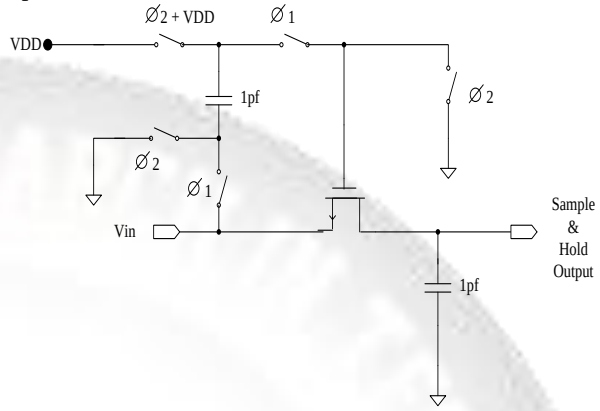


Fig. 3: Sample and Hold circuit

The circuit shown below discusses about the sample and hold operation and the results of it.

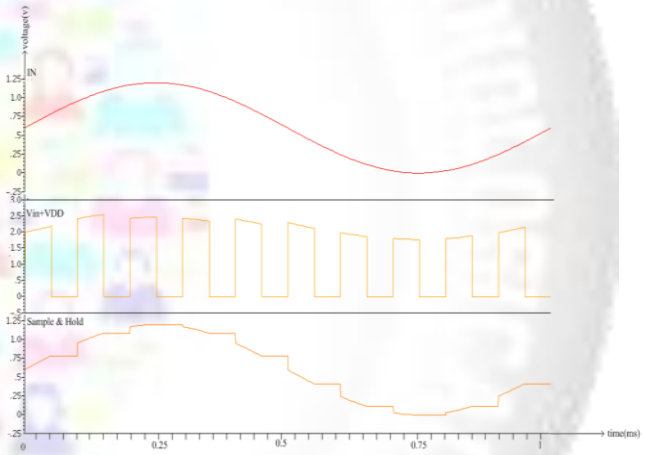


Fig. 4: Waveforms of Input voltage and Sample and Hold output

## IV. Sub-Adc

The main function of the sub-ADC is to provide a digital word corresponding to the input signal or sample of any individual stage. This 1.5 bits/stage design requires the sub-ADC to output 1 of 3 binary states: 00, 01 and 10. The input sample is compared to two thresholds Vref+ and Vref-. Note the nominal thresholds are designed to be at VC -125mV [4]. Also note the actual thresholds may vary from the nominal. However this variance will not affect the final output because the error will be corrected when sent to the following stage. Since the accuracy is not affected by threshold placement, the constraints of the differential comparators are relaxed.

In each sub-ADC there are two differential comparators. The first compares the sample to the Vcm-125mV threshold and the second differential comparator compares the sample to the Vcm+125mV threshold. The input voltage varies between Vcm500mV. The combined outputs of the differential comparators are 00 if Vin ≤

(Vcm-125mV ) , 01 if (Vcm-125mV ) ≤ Vin ≤ (Vcm+125mV ) and 10 if Vin ≥ (Vcm+125mV ). The outputs of these differential comparators are then sent to a sub-DAC block and to the correction logic block [6].

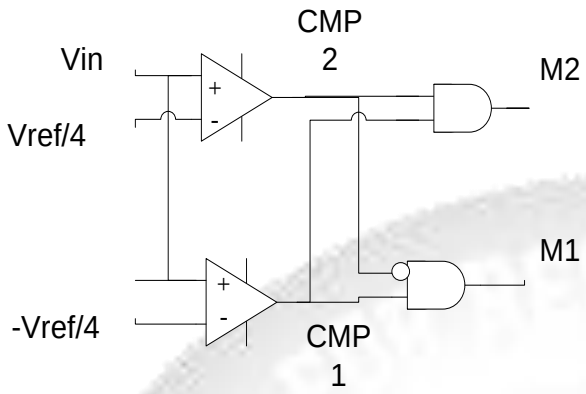


Fig. 5: Schematic of Sub-ADC

| Case | VIN | CMP2 | CMP1 | M2 | M1 |
|---|---|---|---|---|---|
| 1 | VIN ≤ -VR/4 | 0 | 0 | 0 | 0 |
| 2 | -VR/4 ≤VIN ≤ VR/4 | 0 | 1 | 0 | 1 |
| 3 | VIN ≥ VR/4 | 1 | 1 | 1 | 0 |

Table1: Sub-ADC outputs

## V. SUB-DAC

Another key component to the each stage is the sub-DAC. The main role of a sub-DAC is to supply the gain stage with an analog voltage level that represents the quantized portion of the input sample [15]. This quantized portion is subtracted from the original signal to create the residue. In this design, as mentioned the sub-DAC not only provides the analog output but also calculates the digital word sent to the digital correction logic circuit. Each stage can output 00, 01 or 10 for a digital word and the corresponding sub-DAC outputs will be -VR, 0 or +VR.

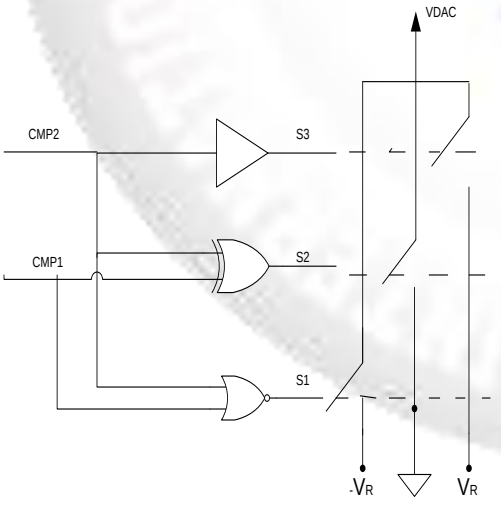


Fig. 6: Schematic of Sub-DAC

| CMP2 | CMP1 | S3 | S2 | S1 | VDAC |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | -VR |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | +VR |

Table2: Sub-DAC outputs

## VI. COMPARATOR

Number of comparators to be used for n-bit Flash ADC are ($2^n$-1).Basic idea of comparator is that it compares held value which is an Output from Bootstrap Switch and to the reference voltage. Output of the comparator is digital logic value either '0' or '1' depending upon the input voltage and reference voltage applied to the comparator as shown in fig7[5]. Output of comparator is logic 1 when input voltage is greater than reference voltage and Output is logic 0 when input voltage is less than reference voltage [12].

### *A. Details of Comparator Architecture:*

We implemented Comparator using a Double-tail latch type voltage sense amplifier [5]. The main advantage of this comparator is that low supply voltage is sufficient to operate it and reset transistors are not required at the output. When clock goes low i.e. 0v, PMOS transistors M7, M8 makes D+ and Di- nodes to precharge to supply voltage i.e. VDD. Since Di inputs are precharged to VDD which makes transistors M10 and M11 turn on which makes the output nodes to discharge to ground i.e. to '0'v. When clock goes high i.e. supply voltage which makes transistors M9 and M12 turn on .Differential input's voltage is developed across the gates of M10 and M11. By taking inputs into consideration, which input voltage is high, for that corresponding output voltage is high. For example if input voltage DIFFIN1 is higher than input voltage DIFFIN2 then output OUT+ is high[14].

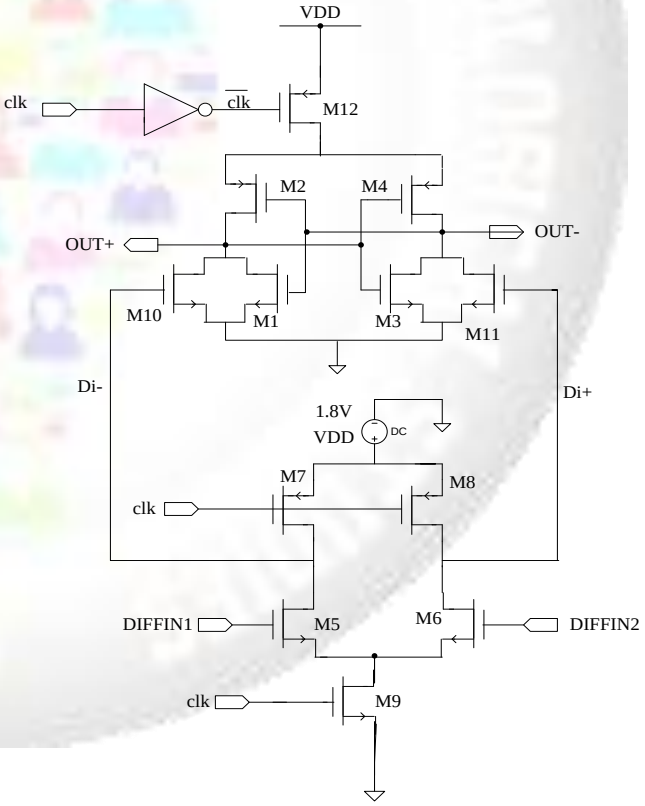


Fig. 7: Comparator with Latch type

We implemented Comparator using a Double-tail latch type voltage sense amplifier. The main advantage of this comparator is that low supply voltage is sufficient to operate it and reset transistors are not required at the output. When clock goes low i.e. 0v, PMOS transistors M7, M8 makes D+ and Di- nodes to precharge to supply voltage i.e.

VDD. Since Di inputs are precharged to VDD which makes transistors M10 and M11 turn on which makes the output nodes to discharge to ground i.e. to '0'v. When clock goes high i.e. supply voltage which makes transistors M9 and M12 turn on .Differential input's voltage is developed across the gates of M10 and M11. By taking inputs into consideration, which input voltage is high, for that corresponding output voltage is high. For example if input voltage DIFFIN1 is higher than input voltage DIFFIN2 then output OUT+ is high.

## VII. Digital Correction Logic

Output of ($2^n$-1) comparators contains string of 1's followed by string of 0's depending upon the location of input. For example say if the input lies between 2nd and 3rd comparators, below the input value, all the comparator output values are 1's and all the comparator will read 0's for above input values. This code is called Thermometer code [11].

Redundancy is always present because in principle if we have input voltage greater than 5th comparator reference voltage then there is no need to compare comparator which is below the 5th comparator. All comparators below the 5th comparators are logic 1's [13].

## 8.SIMULATION RESULTS

The Simulation results are as shown.

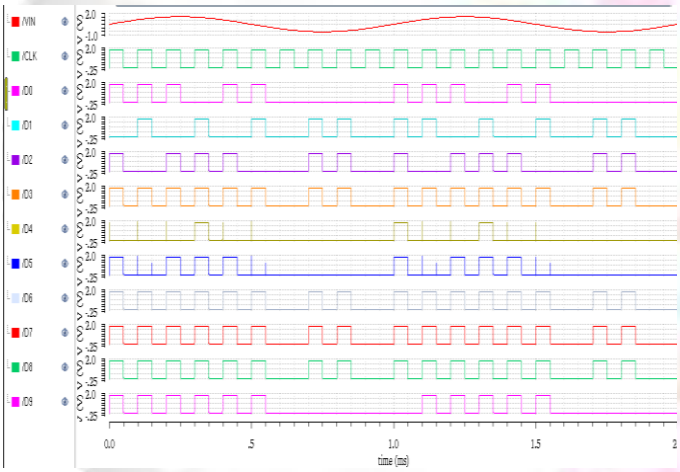

Fig. 8: Output of 10-bit pipelined ADC

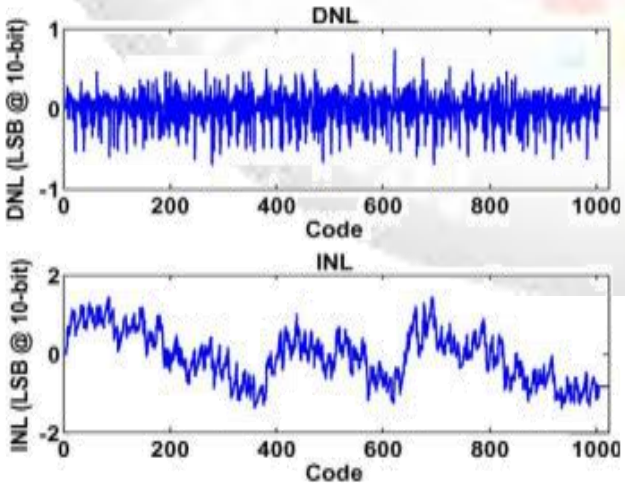


Fig. 9: DNL and INL of 10-bit pipelined ADC

| Parameters | [1] | [11] | [7] | This Work |
|---|---|---|---|---|
| Process | 130nm | 45nm | 180nm | 45nm |
| Sampling Rate (MS/s) | 25 | 120 | 20 | 40 |
| Resolution (bit) | 10 | 10 | 12 | 10 |
| Power(mw) | 1.25 | 61.6 | 17.2 | 1.14 |
| Op-amp type | Gm-based | Folded Cascode | Split-CLS, ZCBC | Differential pair |

Table 3: Comparison with pipelined ADC architecture

## VIII. Conclusion

The design of 1v, 10-bit pipeline ADC is implemented in Cadence Virtuoso Schematic editor using CMOS 45nm technology. The overall design is tested with various input signals and the results obtained are satisfactory. The ADC accepts a full-scale differential input signal of 2V peak to peak and has a differential capacitive loading of 2pF. The DNL and INL plots are shown in fig.11. The measured Differential non linearity is 0.5/LSB and integral non linearity is 0.6/LSB. The designed 10-bit pipelined ADC is working for 10 MHz input frequencies and the maximum sampling rate archived from the design is 40Ms/s.

## References

[1] Amplifier Yunjae Suh, Jongmi Lee, Byungsub Kim, Hong-June Park, And Jae-Yoon Sim ,"A 10-Bit 25-Ms/S 1.25-Mw Pipelined Adc With A Semidigital Gm-Based Amplifier"

[2] J. Hu, N. Dolev, And B. Murmann, "A 9.4-Bit, 50-Ms/S, 1.44-Mw Pipelined Adc Using Dynamic Source Follower Residue Amplification," Ieee J. Solid-State Circuits, Vol. 44, No. 4, Pp. 1057–1066, Apr. 2009.

[3] I. Ahmed, J. Mulder, And D. A. Johns, "A Low-Power Capacitive Charge Pump Based Pipelined Adc," Ieee J. Solid-State Circuit, Vol. 45, No. 5, Pp. 1016–1027, May 2010.

[4] D.-W. Jee, S.-J. Park, H.-J. Park, And J.-Y. Sim, "A Low-Voltage Opamp With Digitally Controlled Algorithmic Approximation," Inproc. Ieee Cicc, 2008, Pp. 499–502.

[5] Daniel Schinkel, Eisse Mensink, Eric Klumperink, Ed Van Tuijl, Bram Nauta, "A Low Offset Double –Tail Latch Type Voltage Sense Amplifier".

[6] B. R. Gregoire And U.-K. Moon, "An Over-60 Db True Rail-To-Rail Performance Using Correlated Level Shifting And An Opamp With Only 30 Db Loop Gain," Ieee J. Solid-State Circuits, Vol. 43, No. 12, Pp. 2620–2630, Dec. 2008.

[7] B. Hershberg, S. Weaver, And U.-K. Moon, "Design Of A Split-Cls Pipelined Adc With Full Signal Swing Using An Accurate But Fractional Signal Swing Opamp," Ieee J. Solid-State Circuits, Vol. 45, No. 12, Pp. 2623– 2633, Dec. 2010.

[8] D.-Y. Chang, "Design Techniq Ues For A Pipelined Adc Without Using A Front-End Sample-And-Hold Amplifier," Ieee Trans. Circuits Syst. I, Reg. Papers, Vol. 51, No. 11, Pp. 2123–2132, Nov. 2004.

[9] Y.-J. Kim, H.-C. Choi, G.-C. Ahn, And S.-H. Lee, "A 12 Bit 50 Ms/S Cmos Nyquist A/D Converter With A Fully Differential Class-Ab Switched Op-Amp,"Ieee J. Solid-State Circuits, Vol. 45, No. 3, Pp. 620–628, Mar. 2010.

[10] Y.-C. Huang And T.-C. Lee, "A 10b 100ms/S 4.5mw Pipelined Adc With A Time Sharing Technique," Inproc. Ieee Isscc Dig. Tech. Papers, 2010,Pp. 300–301.

[11] Y.-J. Kim, K.-H. Lee, S.-H. Ji, Y.-G. Kwon, S.-H. Lee, K.-J. Moon, M. Choi, H.-J. Park, And B.-H. Park, "A 10b 120ms/S 45nm Cmos Adc Using A Re-Configurable Three-Stage Switched Op-Amp," Inproc. Ieee Cicc, 2010, Pp. 1–4.

[12] J. Brunsilius, E. Siragusa, S. Kosic, F. Murden, E. Yetis, B. Luu, J. Bray, P. Brown, And A. Barlow, "A 16b 80ms/S 100mw 77.6db Snr Cmos Pipeline Adc," Inproc. Ieee Isscc Dig. Tech. Papers, 2011,Pp. 186–188.

[13] B. Peng, G. Huang, H. Li, P. Wan, And P. Lin, "A 48-Mw, 12-Bit, 150-Ms/S Pipelined Adc With Digital Calibration In 65nm Cmos," Inproc. Ieee Cicc, 2011, Pp. 1–4.

[14] P. Huang, S. Hsien, V. Lu, P. Wan, S.-C. Lee, W. Liu, B.-W. Chen, Y.-P. Lee, W.-T. Chen, T.-Y. Yang, G.-K. Ma, And Y. Chiu, "Sha-Lesspipelined Adc With In Situ Background Clock-Skew Calibration,"Ieee J. Solid-State Circuits, Vol. 46, No. 8, Pp. 1893–1903, Aug. 2011.

[15] K.-H. Leeet Al., "A 12b 50 Ms/S 21.6 Mw 0.18 Mm Cmos Adc Maximally Sharing Capacitors And Op-Amps," Ieee Trans. Circuits Syst. I, Reg. Papers, Vol. 58, No. 9, Pp. 2127–2136, Sep. 2011.

[16] B. D. Sahoo And B. Rasavi, "A 10-Bit 1-Ghz 33-Mw Cmos Adc," In Proc. Ieee Symp. Vlsi Circuits, 2012, Pp. 30–31.