FPGA Based Rockectio Interfacing

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Abstract—*This paper titled "FPGA BASED ROCKET I/O INTERFACE" is aimed for developing and implementation of algorithm for higher rate data transmission for EW receiver interface. In EW technology requires transferring a huge amount of data across the subsystems. The existing FPGA based devices are capable to transmit data of only 150Mb/s to 350Mb/s. So to transmit a giga bit rate of data from one subsystem to another subsystem having FPGAs needs rocket I/O interface. Rocket I/O is such interface which can support transmission rate of 3.125 GB/s. So it is also called Multigigabit Transceiver (MGTs).In this paper the main proposal is to getting higher transmission rates via interfacing rocket I/O subsystems in between of two boards having FPGAs. For interfacing rocket I/O it is very complicated as the data has to be converted into serial data from parallel one (serialization) in transmitter end and again it has to be converted from serial to parallel (de-serialization) in the receiver end and also clock recovery has to be done in both the end. A rocket I/O or Multi-Gigabit transceivers (MGTs) are flexible units for off-chip and has high-speed serial links. It is easy to communicate with other hardware. Simulation of the algorithm will be first done in MATLab then implemented on FPGA with VHDL.The completion of this simulated EW technology based project will enhance the capability of EW Receiver.*

Keywords: -FPGA, AURORA Protocol, Serial and Parallel Communication.

I. INTRODUCTION

Serial transmission [1] engineering is progressively utilized for the transmission of computerized Data because of its enhanced indicator uprightness and high transmission speeds. Serial information transmission intimates that one bit is sent after an alternate on a solitary transmission line. Serial information transmission is suitable for correspondence between two members and also between a few members. Rapid Serial transmission picked up its essentialness on the grounds that parallel I/O plans arrive at physical confinements when information rates start to surpass only 1 Gb/s and can no more give a dependable, savvy implies for keeping signs synchronized. Serial I/O-based[5] outlines offer numerous points of interest over parallel usage including fewer gadget pins, decreased board space prerequisites, fewer printed circuit board (PCB) layers, more modest connectors, less demanding design of the PCB, easier electromagnetic obstruction, and better clamor insusceptibility.

Multi-Gigabit Transceiver (MGT)[4] is a Serialiser/Deserialiser (SerDes) equipped for working at serial bit rates over 1 Gigabit/second. Mgts are utilized progressively for information interchanges in light of the fact that they can run over more separations, use fewer wires, and accordingly have easier costs than parallel interfaces with proportional information throughput. MGTs are hard silicon exhibit inside the FPGA. MGTs use diverse new advances to work at high line rates moreover serialization and deserialization. For example, differential indicating, MOS current mode rationale (MCML), accentuation, stage bolted circles (PLLs), mistake recognition, channel holding and Electrical Idle/Out-of-Band Signaling. As FPGAs build in size and execution, I/O assets turn into the principle bottleneck to FPGA execution. In spite of the fact that the successful zone of a chip develops as the square of the characteristic size, the edge I/Os develop just directly. State of the symbolization plans obliges higher execution I/O modules. In light of this

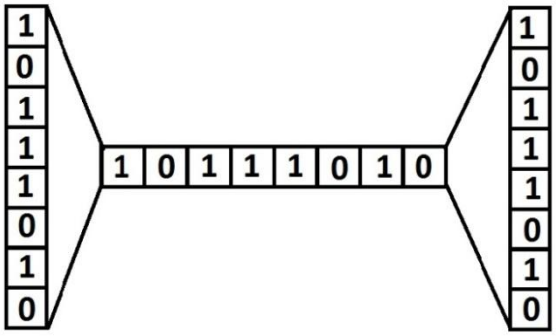

Fig.1: Parallel transmission to serial transmission and again serial transmission to parallel transmission

expanding request on I/O assets, Xilinx has created novel I/O structures called Rocket I/O™ multi gigabit transceivers (MGTs) that empower request of-greatness expands in I/O execution. The Rocket I/O MGTs twofold the aggregate I/O transmission capacity of the Virtex-II Pro™ group of gadgets utilizing just a couple of percent of the pins. With up to 16 MGTs for every gadget, the Virtex-II Pro accomplishes an extra 100 gigabits for every second of I/O transmission capacity in the bigger gadgets over what is accessible with the universally useful I/O squares. Rocket I/O MGTs empower different gigabit I/O gauges and augment execution for FPGA-to-FPGA interchanges. Despite the fact that Rocket I/O MGTs significantly build execution for requesting provisions, they are simple enough to use for basic FPGA-to-FPGA correspondences with extraordinary delicate macros, for example, the Aurora center accessible from Xilinx. The interface has been streamlined to the degree that no outside resistive end is needed with the Rocket I/O MGTs. The transceivers could be inside arranged to match 50_ or 75_ transmission lines.

Obviously, Virtex-II Pro Platform FPAs with Rocket I/O Mgts provide for you favorable element, both as far as execution and time to market. On the other hand, numerous Mgts might be fortified together to structure a higher-transfer speed interface. The Aurora macro guarantees that channel-reinforced information will show up on the same time cycle at the flip side of the interchanges join. The 8b/10b encoding system is utilized for the Aurora delicate macro, giving a powerful data transmission of 10 gigabits for every second for a set of four channel reinforced MGTs between two FPGAs.

II. EXSISTING METHODS

Awhile ago the parallel transmission engineering was utilized for transmitting 128 bit parallel information. Information is transmitted as four 32 bit parallel information, utilizing multiplexer as a part of this innovation. In this arrangement 32 parallel lines are utilized for transmitting and getting information which would devour more assets and time taking methodology when contrasted with serial transmission.

III. PROPOSED METHODS

Aurora is a range productive, adaptable information exchange convention for high velocity serial connections. There are two sorts of aurora convention relying upon the kind of encoding and decoding. They are

- Aurora 8b/10b protocol
- Aurora 64b/66b protocol

The Aurora 8b/10b protocol[1] is utilized as a part of the execution of the application. It is a scalable, link-layer protocol that could be utilized to move information from point-to-point over one or all the more high velocity serial paths (Lane is a full duplex physical serial connection). The Aurora 8b/10b is protocol autonomous and might be utilized to transport industry standard protocols, for example, Ethernet and TCP/IP, or exclusive protocols. This permits architects of cutting edge correspondence and registering frameworks to attain higher network execution. The Aurora 8b/10b protocol is basically focused at chip-to-chip and board-to -board applications and it can additionally be utilized for box-to-box provisions with the expansion of standard optical interface segments. It is an open standard and is accessible for execution by anybody without restriction.

Xilinx has created a product macro called the Aurora center that gives simple 16-bit and 32-bit interfaces from FPGA-to-FPGA utilizing one or more Rocket I/O MGTs. The Aurora core handles the framing, synchronization, and channel bonding tasks, permitting you to center all the more on their provision. A solitary MGT can give a 16-bit or 32-bit FPGA-to-FPGA interface. The product Aurora center coupled with hard core (actualized in silicon) MGTs can make influential serial-to-parallel and parallel-to-serial transceivers. Then again, numerous MGTs could be reinforced together to structure a higher-bandwidth interface. The Aurora macro guarantees that channel-reinforced information will show up on the same time cycle at the flip side of the correspondences join. The 8b/10b encoding technique is utilized for the Aurora delicate macro, giving a compelling transfer speed of 10gigabits for every second for a set of four channel reinforced MGTs between two FPGAs.

The LogiCORE IP[8] Aurora 8b/10b core actualizes the Aurora 8b/10b protocol utilizing the fast serial transceivers on the Virtex-5 LXT, FXT, SXT and TXT family, the Virtex-6 CXT, HXT, LXT, SXT and easier control family, and the Spartan-6 LXT crew. The Aurora 8b/10b center is a lightweight, serial interchanges convention for multi-gigabit links. It is utilized to exchange information between gadgets utilizing one or numerous GTP/GTX transceivers. Associations might be full-duplex (information in both headings) or simplex.

Aurora 8b/10b cores naturally introduce a channel when they are joined with an Aurora channel accomplice. After initialization, applications can pass information openly over the channel as edges or streams of data. Aurora frames could be any size, and might be interrupted at whatever time. Gaps between legitimate information bytes are consequently loaded with unmoving successions to keep up lock and avert over the top electromagnetic interference. Flow control is discretionary in Aurora and could be utilized to diminish the rate of approaching information, or to send short high necessity messages through the channel.

Streams are executed in the Aurora 8b/10b center as a solitary, unending frame. At whatever point information is not being transmitted, unmoving groupings are transmitted to keep the connection alive. The Aurora 8b/10b center recognizes single-bit, and most multibit errors utilizing 8b/10b coding principles. Unreasonable bit failures, disengagements, or supplies disappointments cause the center to reset and endeavor to re-instate another channel.

The Aurora 8b/10b protocol portrays the exchange of client information over an Aurora 8b/10b channel. An Aurora 8b/10b channel comprises of one or more Aurora 8b/10b lanes. Every Aurora 8b/10b lane is a full-duplex serial information association. The gadgets that impart over the channel are called channel partners.

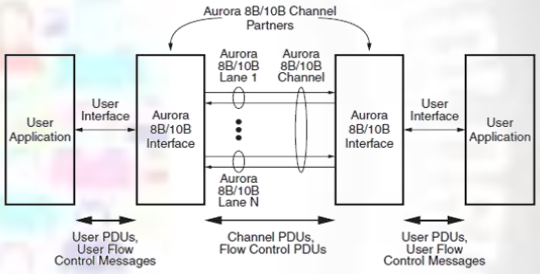

Fig.2: Aurora protocol characteristics

In the figure-2, it demonstrates that how the communication between two user applications through aurora cores. It additionally demonstrates that the aurora paths and channels where the serial transmission of the information is transmitted between the users.

IV. IMPLEMENTATION OF FPGA

A. Software resources:

1. Xilinx 13.2 ISE tool
2. Xilinx core generator
3. Xilinx aurora protocol
4. Hardware Resources:
5. Virtex-6 RocketIO development board.
6. SFP transceiver
7. Optical fiber cable
8. Switch Mode Power Supply (SMPS)
9. JTAG cable

The Xilinx FPGA device used is virtex-6 LX series (XCV6LX195T-2FF1156) with speed grade -2 and package ff1156. It is used for the logic implementation of high speed serial connectivity.

The different platforms in which virtex6 devices present are LX, LXT, SXT, TXT and FXT platforms. Every

one is determined for specific reason relying upon the requisition.

- Virtex-6 LXT FPGAs: High-execution logic with cutting edge serial network.
- Virtex-6 SXT FPGAs: Highest signal processing capability with cutting edge serial capability.
- Virtex-6 HXT FPGAs: Highest transfer speed serial integration.

Gigabit transceivers are available inside the FPGA silicon. GTP and GTX are the two sorts of transceivers present in the virtex6. Rocketio GTP transceivers are available in LXT and SXT Platforms which backings speeds in the extent of 100 Mb/s to 3.75 Gbps baud rates. RocketIO GTX transceivers are available in HXT Platform which backings speeds in the reach of 150 Mb/s to 6.5 Gbps baud rates. Every transceiver backings full-duplex, check and information recuperation in virtex-6 series.

RocketI/Os are used for high speed serial data transfer. They are multigigabit Transceiver (MGTS). They enable high speed interfaces for Virtex-II Pro Platform FPGAS. For best purpose here AURORA protocol is used. The advantages of using Aurora protocol is it is highly flexible for transmitting huge amount of data in FIFO condition. But the disadvantage is ACK signal cannot be traced in here.

The application is implemented in the following Phases

1. COUNTER implementation phase
2. AURORA Protocol Implementation phase using Multi-Gigabit transceivers.

1) Counter Implementation phase:

A binary counter is designed with 128 bits width and it counts up to 128 and starts from zero. The counter is designed by using combinational logic, VHDL code is written to generate the required output. Synthesis, simulation and implementation of the code are done using Xilinx ISim[7] (ISim is an abbreviation for ISE Simulator, an integrated HDL simulator used to simulate Xilinx FPGA and CPLD designs)[4] and chip scope PRO analyzer.

2) Aurora protocol implementation phase with the use of multi gigabit transceivers:

Multi-gigabit transceivers are present in FPGA as hard silicon. These are configured using aurora protocol for the application of high speed serial data transmission at the rate of 3.125 GHz of high speed serial data transmission.

B. Customizing Aurora core:

One of the vital parameters that we ought to select while creating the center is Lane Width which chooses the amount of bytes transmitted throughout the time of one clock cycle. Aurora helps Lanewidth of 2 and 4. In the event that we set the Lanewidth to 4, the client clock (USER CLK) ought to be a large portion of the reference clock (REFCLK), while with a Lanewidth of 2, the recurrence of USER CLK and REFCLK ought to be the same. In this way, the powerful information rate will be same for both cases. Besides, the clock era for a Lanewidth of 4 is entangled than for a Lanewidth of 2. So we have chosen the default Lanewidth estimation of 2. There are two sorts of information way interfaces utilized for the center which are Framing and Streaming. Framing interface is basically Local Link interface which allows data encapsulation of any length. Whereas streaming interface is a basic word-based interface with a valid data signal for data streaming through the aurora channel. As in this project the data transmission is continuous over the communication stream, so the best option of selection is streaming. For Aurora core it has two data flow modes. One is Simplex and another Duplex. Here Duplex mode is selected as data transmission is in both directions. To drive the RocketIO transceivers Aurora core supports several clock inputs. Here REFCLK is used as it is low jitter differential clock which supports line rates up to 3.125 Gb/s. It is selected to match the transceivers clock. Now, select the MGT tile whose connections are brought outside to connect SFP module case for data transmission.

The counter_fifo module is integrated with aurora module. The output of the counter_fifo[9] module is given to the aurora module as input data. The multi-gigabit transceivers which are configured using aurora 8b/10b protocol converts the 2 byte data into 20 bits(each byte-8 bits in to 10 bits). Now these bits of data are converted in to serial form and then transmitted through optical fiber cable using SFP module at the rate of 3.125Gbps (156.25MHz × 20bits). The final integrated module is simulated and the required output is obtained. After implementation process in Xilinx ISE the bit file is generated. This bit file is dumped into FPGA using JTAG cable and the results of the logic is observed in chipscope logic analyzer (Software logic analyzer) .

C. SFP Transceiver:

SFP or Small Form Factor Pluggable transceiver is used for both data and tele communication applications. It is a compact and hot-pluggable transceiver. It is used to interface network device mother board with fiber optic or copper networking cable. SFP transceivers support Gigabit Ethernet, SONET and Fiber Optic Channel. The module which is completely passive has a minimal effect upon serial data traffic.

SFP transceivers can be available in a variety of different transmitter and receiver types. It allows user for selecting the appropriate transceiver of each link. Like that it provides to choose available optical fiber type (multiple or single mode fiber). Optical SFPs are of four types- 850nm, 1310nm, 1550nm and DWDM. It is also available with copper cable interface, which allows preliminary in optical fiber communications and also communication through twisted pair networking cable. The optical transceiver which is utilized backings rapid serial connections over multimode optical fiber at indicating rates up to 4.25 Gb/s.SFP transceivers converts the electrical signal to light signal and vice versa.

D. JTAG Cable:

JTAG cable is used for boundary scanning of the FPGA device and communication link between the computer and FPGA board. The full type of JTAG is Joint Test Action Group on the grounds that it is created by Joint Test Action Group and Sanctioned by IEEE as STD 1149.1 test access port and Boundary Scan Architecture in 1990.

E. BIT Files:

Xilinx FPGA configuration files are called Bit files. It sis generate by Xilinx FPGA design software. It contains

configuration information in proprietary format binary form. In the JTAG boundary scan for each Xilinx FPGA at least one Bit file is required.

V. CHIPSCOPE PRO ANALYSER

Chip Scope Pro[2] is programming based logic analyzer .It permits checking the status of the chose motions in a configuration to discover conceivable outline failures. It gives a few centers that might be added to an outline by producing the centers with the CORE Generator apparatus, instantiating them into the source code, and joining the centers to the configuration before the union methodology. Then again, it is conceivable to alter the centers and addition them into the outline net rundown utilizing the Chip Scope Pro Core Inserter apparatus after the combination process. The outline is then executed into the FPGA gadget utilizing the execution apparatuses of the Xilinx. The sort of centers needed for utilizing Chip Scope Pro analyzer are,

1. Symbol (Integrated Controller)
2. ILA (Integrated Logic Analyzer) and
3. VIO (Virtual Input/Output)

Recreation based system is generally utilized for debugging the FPGA plan on workstations. Time needed for recreating complex configuration for all conceivable experiments gets to be restrictively vast and reproduction methodology fizzles. For fast testing, such outlines could be stacked on to the target FPGAs and tried by applying test inputs and straightforwardly watching their yields. As the unpredictability of the outline under test builds, so does the impracticality of appending test supplies tests to these gadgets under test. The ChipscopePro[3] devices incorporate key rationale analyzer and other test and estimation equipment parts with the target outline inside the FPGA. Workstation based programming apparatus correspond with these equipment parts and give a creator hearty rationale analyzer result.

VI. RESULTS

The following are the results obtained for the final integrated FIFO_AURORA module in chipscope analyser.

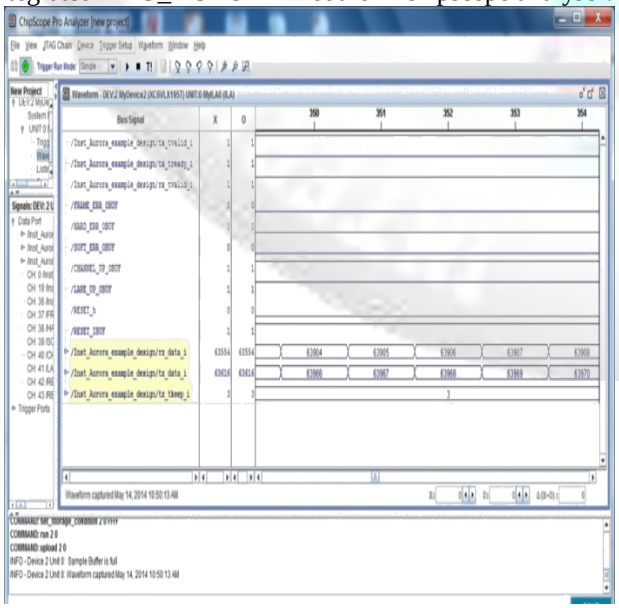

Fig.3: First set of results for input of 63554 rates

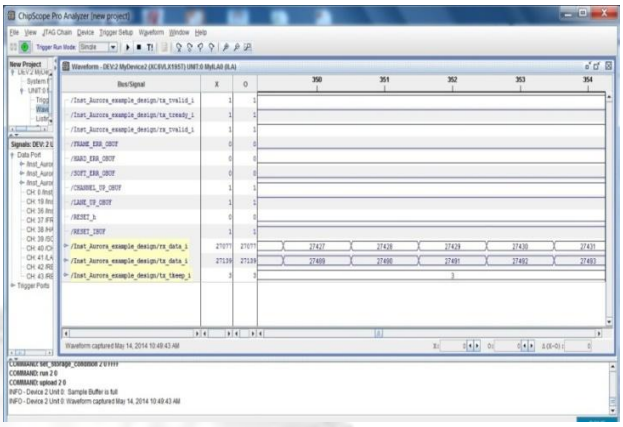

Fig.4: Second set of results for input of 27077 rates

VII. CONCLUSIONS AND FUTURE SCOPE

The high speed serial data is transmitted through optical fiber cable at the rate of 3.125 Gbps using multi-gigabit transceiver and received by other multi-gigabit transceivers. Both the transmitted and received data are monitored in the chip scope analyzer.

The present paper is implemented using aurora protocol for serial data transmission of rate of 3.125Gbps. The following level convention is Serial Rapid IO (SRIO) which takes a shot at the standard of information bundles exchanging is more effective for failure free transmission and pace might be expanded to larger amount.

ACKNOWLEDGEMENT

My sincere thanks to my internal guide Mr. C.H. Pamuleti, Associate Professor, ECE, SNIST for the encouragement and guidance provided. I am also grateful to Dr. Venumadhao Rao, Head of the Department, ECE, SNIST for his continuous support and valuable guidance. I am also thankful to Dr. Narseema Rao Reddy, Director, SNIST for his valuable guidance.

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