# Implementation of Low Power Test Pattern Generator in BIST Schemes

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***Abstract***— *This paper presents a novel test pattern generator which is more suitable for built in self-test (BIST) structures used for testing of VLSI circuits. The objective of the BIST is to reduce power dissipation without affecting the fault coverage. The proposed test pattern generator reduces the switching activity among the test patterns at the most. In this approach, the single input change patterns generated by a counter and a gray code generator are Exclusive–OR with the seed generated by the low power linear feedback shift register [LP-LFSR]. The proposed scheme is evaluated by using, a synchronous pipelined in the 4x4 and 8x8 Braun array multipliers. The System-On-Chip (SOC) approach is adopted for implementation on Altera Field Programmable Gate Arrays (FPGAs) based SOC kits with Nikos II soft-core processor. From the implementation results, it is verified that the testing power for the proposed method is reduced by a significant percentage.*

**Keywords—** FPGA, BIST, LP-LFSR, Switching activity

## I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation for VLSI circuits [1]. The ability to design, fabricate and test Application Specific Integrated Circuits (ASICs) as well as FPGAs with gate count of the order of a few tens of millions has led to the development of complex embedded SOC. Hardware components in a SOC may include one or more processors, memories and dedicated components for accelerating critical tasks and interfaces to various peripherals. One of the approaches for SOC design is the platform based approach. For example, the platform FPGAs such as Xilinx Virtex II Pro and Altera Excalibur include custom designed fixed programmable processor cores together with millions of gates of reconfigurable logic devices.

In addition to this, the development of Intellectual Property (IP) cores for the FPGAs for a variety of standard functions including processors, enables a multimillion gate FPGA to be configured to contain all the components of a platform based FPGA. Development tools such as the Altera System-On-Programmable Chip (SOPC) builder enable the integration of IP cores and the user designed custom blocks with the Nios II soft-core processor. Soft-core processors are far more flexible than the hard-core processors and they can be enhanced with custom hardware to optimize them for specific application. Power dissipation is a challenging problem for today's System-on-Chips (SOCs) design and test.

In general, the power dissipation of a system in test mode is more than in normal mode [2]. Four reasons are blamed for power increase during test [3].

- High switching activity due to nature of test patterns
- Parallel activation of internal cores during test
- Power consumed by extra design-for-test (DFT) circuitry
- Low correlation among test vectors

This extra average and peak power consumption can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product field and life time[4]. Thus special care must be taken to ensure that the power rating of circuits is not exceeded during test application. Different types of techniques are presented in the literature to control the power consumption. These mainly includes algorithms for test scheduling with minimum power, techniques to reduce average and peak power, techniques for reducing power during scan testing and BIST (built-in-self- test) technique. Since off-chip communication between the FPGA and a processor is bound to be slower than on- chip communication, in order to minimize the time required for adjustment of the parameters, the built in self-test approach using design for testability technique is proposed for this case. The rest of the paper is organized as follows. In section II, previous works relevant to power reduction are discussed, which mainly concentrated to reduce the average and peak power. In section III, an overview of power analysis for testing is presented. In section IV, Braun array multiplier is discussed briefly, which is taken here as a circuit under test (CUT) to verify the effectiveness of the proposed technique. In Section V, the proposed technique in the test pattern generator is discussed. Section VI describes the algorithm for the proposed LP-LFSR. In section VII, the implementation details and the results are presented. Section VIII summarizes the conclusion.

## II. REVIEW OF PREVIOUS WORK

Different techniques are available to reduce the switching activities of test pattern, which reduce the power in test mode. For linear feedback shift register (LFSR), Giard proposed a modified clock scheme in which only half of the D flip-flops works, thus only half of the test pattern can be switched [7]. S.K. Guptha proposed a BIST TPG for low switching activity in which there is d-times clock frequency between slow LFSR and normal LFSR and thus the test pattern generated by original LFSR is rearranged to reduce the switch frequency. LT-TPG is proposed to reduce the average and peak power of a circuit during test [4]. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR).

A better low power can be achieved by using single input change pattern generators. It is proposed that the combination of LFSR and scan shift register is used

to generate random single input charge sequences [9] & [10]. In [10 &11], it is proposed that (2m-1) single input change test vectors can be inserted between two adjustment vectors generated by LFSR, m is length of LFSR. In [5], it is proposed that $2^m$ single input changing data is inserted between two neighboring seeds. The average and peak power are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high.

## III. ANALYSIS OF POWER FOR TESTING

In CMOS technology, the power dissipation can be classified into static and dynamic. Static power dissipation is mainly due to the leakage current. Dynamic power dissipation is due to switching transient current and charging and discharging of load capacitances. Some significant parameters for evaluating the power consumption of CMOS circuits are discussed below.

$$E_i = V_d^{\,2} C F S \qquad (1)$$

Where $V_{dd}$ is the supply voltage, C0 is the load capacitance. The product of Fi and Si is called weighted switching activity of internal circuit node i.

The average power consumption of internal circuit node i can be given by,

$$P_i = V d^{\,2} C F S f \qquad (2)$$

F is the clock frequency .The summary of Pi of all the nodes is named as average power consumption. It can be observed from (1) and (2) that the energy and power consumption mainly depends on the switching activities, clock frequency and supply voltage. This paper reduces the switching activity at the inputs of the circuit under test (CUT) as low as possible.

### *A. BIST approach:*

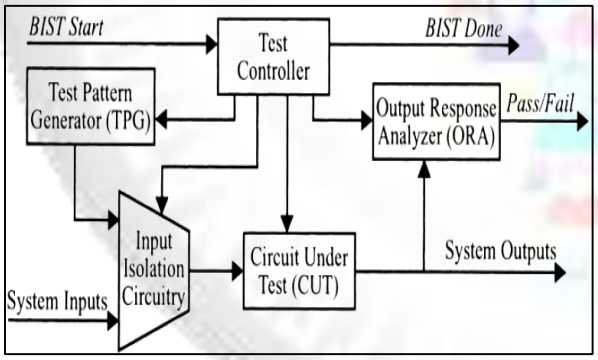


Fig. 1 BIST Basic block diagram

BIST is a design for testability (DFT) technique in which testing is carried out using built –in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture shown in fig.1 needs three additional hardware blocks such as a pattern generator, a response analyzer and a test controller to a digital circuit. For pattern generators, we can use either a ROM with stored patterns, or a counter or a linear feedback shift register (LFSR).A response analyzer is a compactor with stored responses or an LFSR used as a signature analyzer. A controller provides a control signal to activate all the blocks.

BIST has some major drawbacks where architecture is based on the linear feedback shift register [LFSR]. The circuit introduces more switching activities in the circuit under test (CUT) during test than that during normal operation [5].It causes excessive power dissipation and results in delay penalty into the design [6].

### *B. Classification of test strategies:*

*1) Weighted Pseudorandom Testing:*

In weighted pseudorandom testing, pseudorandom patterns are applied with certain 0s and 1s distribution in order to handle the random pattern resistant fault undetectable by the pseudorandom testing. Thus, the test length can be effectively shortened.

*2) Pseudo exhaustive Testing:*

Pseudo exhaustive testing divides the CUT into several smaller sub circuits and tests each of them exhaustively. All detectable flaws within the sub circuits can be detected. However, such a method involves extra design effort to partition the circuits and deliver the test patterns and test responses. BIST is a set of structured-test techniques for combinational and sequential logic, memories, multipliers, and other embedded logic blocks. BIST is the commonly used design technique for self-testing of circuits.

*3) Pseudorandom Testing:*

Pseudorandom testing involves the application of certain length of test patterns that have certain randomness property. The test patterns are sequenced in a deterministic order. The test length and the contents of the patterns are used to impart fault coverage.

*4) Exhaustive Testing:*

Exhaustive testing involves the application of all possible input combinations to the circuit under test (CUT). It guarantees that all detectable faults that divert from the sequential behavior will be detected. The strategies are often applied to complex and well isolated small modules such as PLAs.

*5) Stored Patterns:*

Stored-pattern approach tracks the pre- generated test patterns to achieve certain test goals. It is used to enhance system level testing such as the power-on self-test of a computer and microprocessor functional testing using micro programs.

## IV. DESIGN OF MULTIPLIER

Multipliers are widely used in DSP operations such as convolution for filtering, correlation and filter banks for multi rate signal processing. Without multipliers, no computations can be done in DSP applications. For that reason, multipliers are chosen for testing in our proposed design. Braun array multiplier is selected among various multipliers as it follows simple conventional method. Also, pipelined Braun array multiplier is selected as it is faster in speed than non-pipelined multiplier. To avoid carry propagation delay at every stage, the carry bits are propagated to the next stage. Finally at the last stage, ripple carry adder is used to get the product term of p4 to p7.

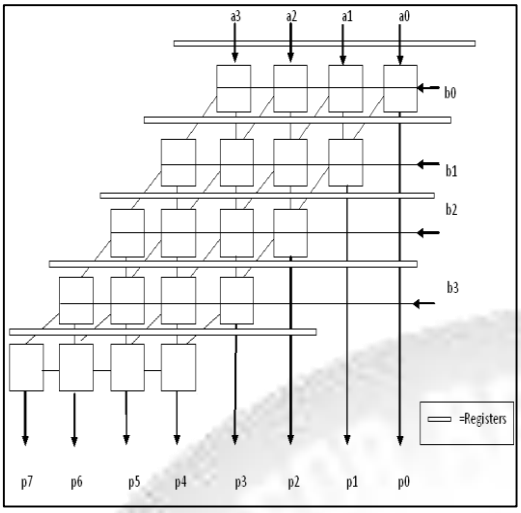


Fig. 2 Braun array multiplier

## V. PROPOSED METHOD

Because of simplicity of the circuit and less area occupation, linear feedback shift register [LFSR] is used at the maximum for generating test patterns. In this paper, we proposed a novel architecture which generates the test patterns with reduced switching activities. LP-TPG structure consists of modified low power linear feedback shift register (LP- LFSR), m-bit counter; gray counter, NOR-gate structure and XOR-array.

The m-bit counter is initialized with Zeros and which generates 2m test patterns in sequence. The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to gray code generator and NOR-gate structure. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied

To activate the LP-LFSR which generates the next seed? The seed generated from LP-LFSR is Exclusive–Oared with the data generated from gray code generator. The patterns generated from the Exclusive–OR array are the final output patterns.

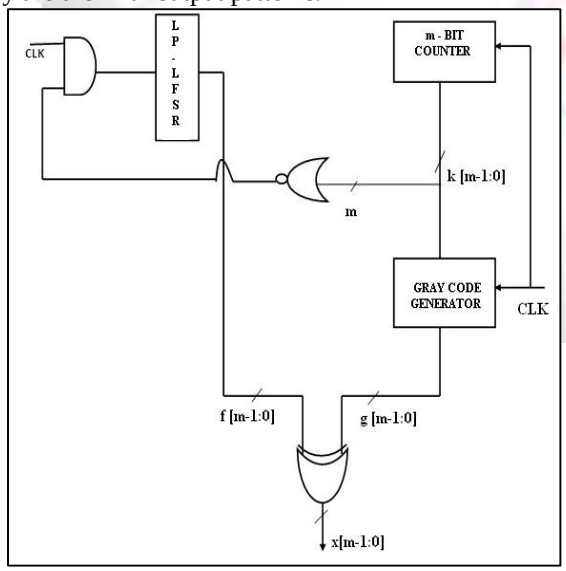


Fig. 3: Low Power Test Pattern Generator

## VI. ALGORITHM FOR LP-LFSR

The algorithm for LP-LFSR is given below:

Consider a N-bit external (or) internal linear feedback shift register [n>2].

- For example n-bit, external LFSR is taken, which consists of n-flip flops in series. A common clock signal is applied as control signal for all flip flops.
- For exchanging the output of adjacent flip flops, multiplexers are used. The output of the last stage flip flop is taken as a select line.
- If the last stage flip flop output is one, any one of the flip flop output is swapped with its adjacent flip flop output value.
- If the last stage flip flop output is Zero, no swapping will be carried out.
- The output from other flip flops will be taken as such.
- If the LFSR is moved through a complete cycle of 2n states then the transitions expected are 2n-1.When the output of the adjacent flip flops are swapped, the expected transitions are 2n-2.Thus the transitions produced are reduced by 50% compared with original LFSR. The transition reduction is concentrated mainly on any one of the multiplexer output.
- Gray converter modifies the counter output such that two successive values of its output are differing in only one bit. Gray converters can be implemented as shown below.

g[n-1]= k [n-1]

g[n-2]= k [n-1] XOR k[n-2]

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g[2]= k [2] XOR k[3]

g[1]= k[1] XOR k[2]

g[0]= k[0] XOR k[1]

In [12] it is stated that that the conventional LFSR's outputs cannot be taken as the seed directly, because some seeds may share the same vectors. Thus the LP-LFSR should ensure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. Test patterns generated from the proposed structure are implemented as following equations. x[0] = f[0] XOR g[0] x[1] = f[1] XOR g[1] x[2] = f[2] XOR g[2] x[3] = f[3] XOR g[3] x[4] = f[4] XOR g[4] x[5] = f[5] XOR g[5]

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X [n-1] = f[n-1] XOR g[n-1]

Thus the XOR result of the sequences is single input changing sequence. In turn reduces the switching activity and so power dissipation is very less compared with conventional LFSR. Fig. 3 is an example of counter and its

respective gray value. It is shown that all values of g[2:0] are single input changing patterns.

Patterns:

| K [2:0] | g [2:0] |
|---|---|
| K0= 000 | g0= 000 |
| K1= 001 | g1= 001 |
| K2= 010 | g2= 011 |
| K3= 011 | g3= 010 |
| K4= 100 | g4= 110 |
| K5= 101 | g5= 111 |
| K6= 110 | g6= 101 |
| K7= 111 | g7= 100 |

## VII. Implementation Details

To validate the effectiveness of the proposed method, we select Test pattern generator (TPG) using conventional linear feedback shift register [LFSR] for comparison with proposed system. Table 1 shows the power consumption comparison between TPG using conventional LFSR and the proposed LP- LFSR after applying the generated patterns to the 4x4 and 8x8

Braun array multipliers respectively. The generated test patterns from above two techniques are used to test the synchronous pipelined 4x4 and 8x8 Braun array multipliers.

| Size | LFSR with 4x4 | LP-LFSR with 4x4 | LFSR with 8x8 | LP-LFSR with 8x8 |
|---|---|---|---|---|
| Logic Elements | 86 | 90 | 176 | 178 |
| Registers | 81 | 81 | 173 | 173 |
| Frequency (MHz) | 132.33 | 132.87 | 393.55 | 401.28 |
| Total power dissipation (mw) | 147.72 | 140.42 | 328.81 | 320.32 |
| Dynamic power dissipation (mw) | 18.45 | 11.34 | 50.68 | 38.32 |
| Static power dissipation (mw) | 80.03 | 80.01 | 80.65 | 80.63 |

Table –1 Comparison Of Power Consumption

Simulation and analysis were carried out with QUARTUS-II 9.1 version. Power play power analyzer tool was used for the Power analysis. The average test power consumption was compared with the test pattern generator (TPG) using conventional LFSR. In table I, the average test power consumption for the TPG using conventional LFSR and the average test power consumption for the proposed LP-LFSR are presented. The test patterns generated from this LP-LFSR is tested with 4x4 and 8x8 Braun array synchronous pipelined multipliers.

The total number of switching transitions in the design is

Shown in table 2. Switching activities for multiple input changing sequence will be more than the single input changing sequence, thus the proposed method provides better test power reduction than any other low power methods.

| Types of Multiplier | Total no. of switching transitions |
|---|---|
| TPG using LFSR with 4x4 Braun array multiplier | 41956 |
| TPG using LP-LFSR with 4x4 Braun array multiplier (proposed) | 41798 |
| TPG using LFSR with 8x8 Braun array multiplier | 126496 |
| TPG using LP-LFSR with 8x8 Braun array Multiplier(proposed) | 121077 |

Table – 2 Total Number of Switching Transitions

From the implementation results, it is verified that the proposed method gives better power reduction compared to the exiting method.

The above LP-LFSR is also tested with In-System memory content editor using Mega wizard plug-in manager available with QUARTUS-II. The same was also verified with NIOS II processor.

## VIII. Conclusion

A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The seed generated from (LP-LFSR) is Ex-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities among the test patterns. Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR in place of conventional LFSR in the circuit used for test pattern generator. From the implementation results, it is verified that the proposed method gives better power reduction compared to the exiting method.

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