Implementation and Analysis of High Speed Multipliers – A Vedic Multipliers Approach

Parachoori Sai Krishna[1] Rayala Sateesh[2]
[1]P.G. Scholar [2]Assistant Professor
[1,2]Sri Rama Institute of Technology and Science

Abstract— *one of the most important arithmetic units in DSPs and microprocessors is multiplier. It is also a major source of power dissipation. To reduce the power dissipation of multipliers is the key to satisfy the overall budget of digital circuits. This paper analyses and compares array multiplier with Vedic multiplier so that we can select a better multiplier design to perform multiplication of two numbers. The main objective of our work is to calculate and compare the total number of LUTs utilized by array and Vedic multipliers. The designs are done using ISE Design Suit 14.4 tool and are simulated using Modelsim as simulator.*

Keywords— Array multipliers, full adder, Vedic multipliers

I. Introduction

Computational performance of a microprocessor or a DSP system is limited by the performance of arithmetic units like adders, comparators and multipliers. Therefore high speed & low power arithmetic core is much desired. Ultimately, binary addition is the most basic operation found in most arithmetic operations. Addition is the most basic arithmetic operation and adder is the most fundamental arithmetic component of the processor. The rest of the paper is organized as follows. Section II describes the array multiplier. Section III elaborates the Vedic multiplier. Section IV and V are followed by comparison and simulation results and conclusion.

II. Array multiplier

Array multiplier is an efficient layout of a combinational multiplier. It uses short wires that go from one full adder to adjacent full adders horizontally, vertically or diagonally. [4] In array multiplier, consider two binary numbers A and B, of m and n bits. There are MN summands that are produced in parallel by a set of MN AND gates. An n x n multiplier requires n (n-2) full adders, n half- adders and n2 AND gates. The shifting of partial products for their proper alignment is performed by simple routing and does not require any logic. The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders. Each row of full adders or 3:2 compressors adds a partial product to the partial sum, generating a new partial sum and a sequence of carries.

Also, in array multiplier worst case delay would be (2n+1) td. Array Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased; due to this array multiplier is less economical .Thus, it is a fast multiplier but hardware complexity is high.

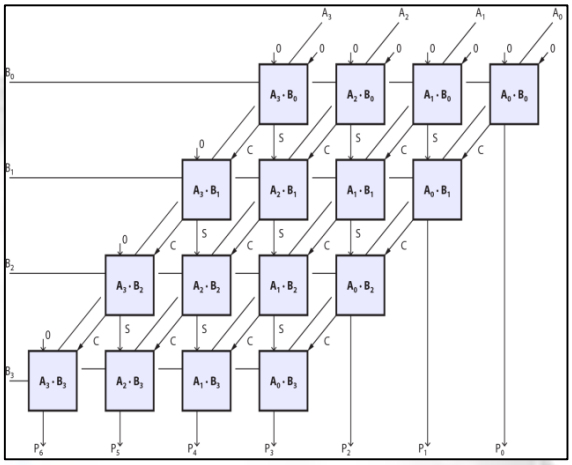


Fig. 1 A 4-Bit Array Multiplier

The delay associated with the array multiplier is the time taken by the signals to propagate through the AND gates and adders that form the multiplication array. Delay of an array multiplier depends only upon the depth of the array not on the partial product width.

III. Vedic multiplication

The word "Vedic" is derived from the word **"Veda"** which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (formulae) and 16 Up-Sutras (sub-formulae) dealing with various branches of mathematics like arithmetic, algebra, geometry etc.[5] These Sutras along with their brief meanings are enlisted below alphabetically.

- (Anurupye) Shunyamanyat: If one is in ratio, the other is zero.
- Chalana-Kalanabyham: Differences and Similarities.
- Ekadhikina Purvena: By one more than the previous One.
- Ekanyunena Purvena: By one less than the previous one.
- Gunakasamuchyah: The factors of the sum are equal to the sum of the factors.
- Gunitasamuchyah: The product of the sum is equal to the sum of the product.
- Nikhilam Navatashcaramam Dashatah: All from 9 and last from 10.
- Paraavartya Yojayet: Transpose and adjust.
- Puranapuranabyham: By the completion or noncompletion.
- Sankalana-vyavakalanabhyam: By addition and by subtraction.
- Shesanyankena Charamena: The remainders by the last digit.

- Shunyam Saamyasamuccaye: When the sum is the same that sum is zero.
- Sopaantyadvayamantyam: The ultimate and twice the penultimate.
- Urdhva-tiryakbhyam: Vertically and crosswise.
- Vyashtisamanstih: Part and Whole.
- Yaavadunam: Whatever the extent of its deficiency.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome- looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. [1, 3]

The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial- parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers.

A. General 2X2 Vedic Multiplier [2]:

The method is explained below for two, 2 bit numbers A and B where A = a1a0 and B = b1b0 as shown in Figure 2. Firstly, the Least Significant Bits are multiplied which gives the Least Significant Bit (LSB) of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

$s0 = a0b0$ -- (i)
$c1s1 = a1b0 + a0b1$ -- (ii)
$c2s2 = c1 + a1b1$ -- (iii)

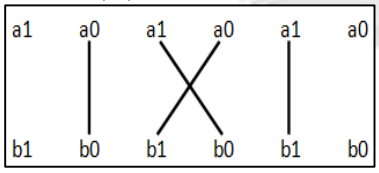


Fig. 2 The Vedic Multiplication Method for two 2-bit binary numbers

The final result will be *c2s2s1s0*. This multiplication method is applicable for all the cases. The 2x2 bit Vedic multiplier (VM) module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Figure 3.

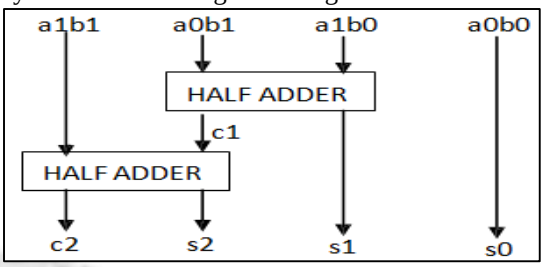
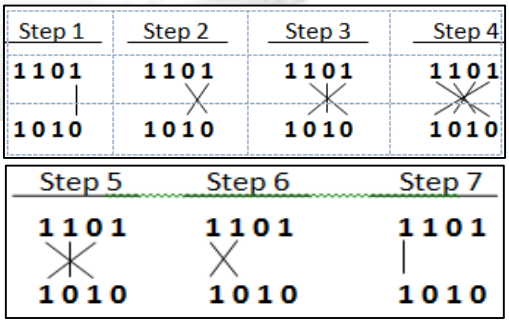


Fig. 4 Using Urdhava Tirkyakbhyam for binary numbers

The same method can be extended for higher no. of input bits (say 4).

B. Urdhva Tiryakbhyam Sutra:

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done and then, concurrent addition of these partial products can be done. Thus parallelism in generation of partial products and their summation is obtained using Urdhava Tiryakbhyam. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. It has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It will enhance the ALU unit also.



C. 4X4 Multiplier Block:

The 4X4 Multiplier is made by using four 2X2

multiplier blocks. The multiplicands are of bit size n=4 where as the result is of 8 bit size. The input is broken into smaller chunks of size n/2= 2, for both inputs, that is a and b. These newly formed chunks of 2 bits are given to 2X2 multiplier block to get the 4 Bit result. The same method is followed for the multipliers of higher bits like 8, 16 and 32 bits.

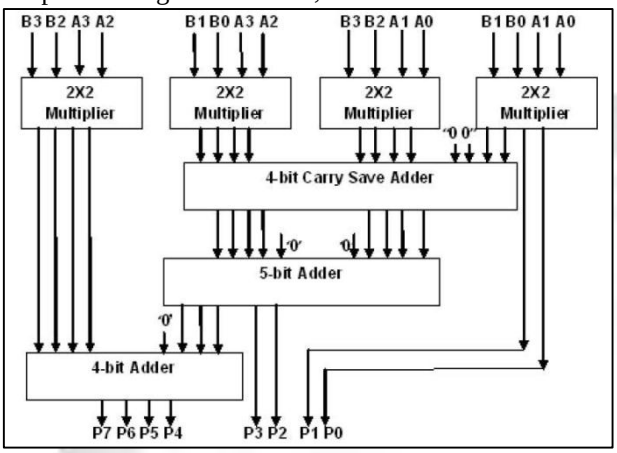


Fig. 5 Block diagram of 4x4 Multiplier Block

The equations of the 4x4 multiplier are: X = a3a2a1a0
Y = b3b2b1b0
P0 = a0.b0
P1 = a1.b0 + a0.b1
P2 = a2.b0 + a1.b1 + a0.b2 + P1(1)
P3 = a3.b0 + a2.b1 + a1.b2 + a0.b3 + P2(2 to1) P4 = a3.b1 + a2.b2 + a1.b3 + P3(2 to 1)
P5 = a3.b2 + a2.b3 + P4 (2 to 1)
P6 = a3.b3 + P5 (2 to 1)
Product = P6 & P5 (0) & P4 (0) & P (3) & P (2) & P (1) & P (0) & - Concatenate

IV. NIKHILAM SUTRA

The example of Nikhilam multiplication is shown in the below figure6. Here the nearest base is chosen first. The multiplicand and the multiplier will be subtracted from the nearest base, which is equivalent to taking two's complement. Then the product of the two's complement and the common difference will give the final result [2].

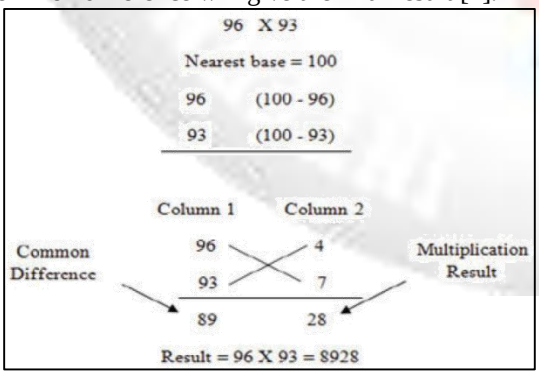
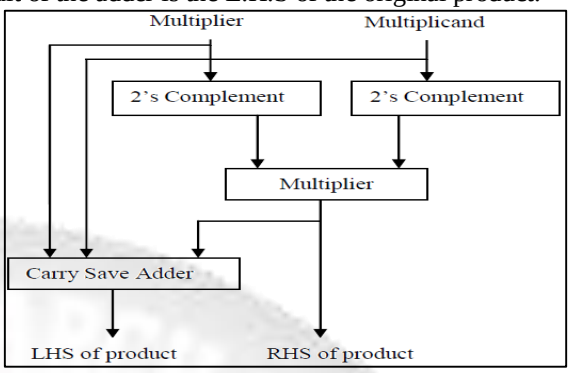


Fig. 6: Multiplication using Nikhilam

The Nikhilam multiplier architecture is shown in the below figure7. Here the two inputs are first complimented and those complimented results are multiplied. Here the multiplier used also plays an important role in calculating delay. We can use either Vedic multiplier or array multiplier. Then the multiplier output is added to the two inputs a and b. The right hand side result of the multiplier is the R.H.S of the original product and the L.H.S result of the adder is the L.H.S of the original product.



V. RESULTS AND CONCLUSION

From above comparison we find that number of LUTs of Urdhava Tiryakbhyam(Vedic multiplier) are less as compared to that of Array multiplier. As such, the area of Vedic multiplier will be lesser to that of Array multiplier. Also, delay of Vedic multiplier will be lesser than Array multiplier. So, performance of Vedic multiplier is better than that of Array multiplier. Hence Urdhava Tiryakbhyam multiplier (Vedic multiplier) is better multiplier compared to Array multiplier when compared to total number of LUTs.

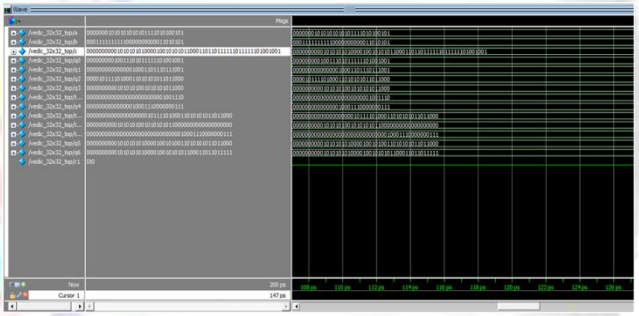


Fig. 8 Simulation Result for 32bit Vedic Multiplier

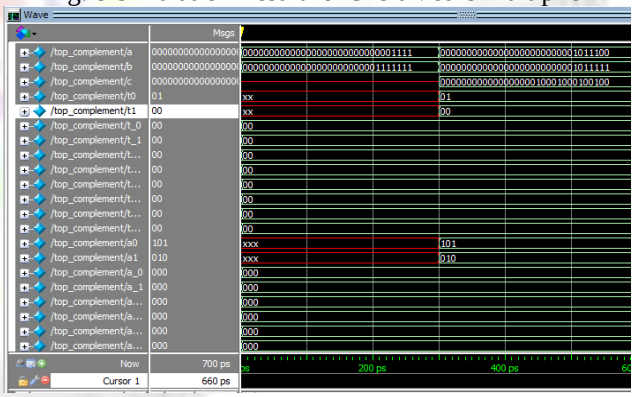


Fig. 9: Simulation Result for 32bit Nikhilam Multiplier

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