Realization of Carry Select Adder using Hybrid Model

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Abstract— highly increasing requirement for mobile & several electronic devices want the use of VLSI which is highly power efficient. The most primitive arithmetic operation in processors is addition and the adder is the most highly used arithmetic component of the processor. Carry Select Adder (CSA) is one of the fastest adders and the structure of the CSA shows that there is a possibility for increasing its efficiency by reducing the power dissipation and area in the CSA. This research paper presents power and delay analysis of various adders and proposed a 32-bit CSA that is implemented using Hybrid PTL/CMOS logic style. The results analysis is showing that the proposed CSA structure shows better result in terms of area, power and PDP (Power Delay Product) than the others.
Keywords— Delay, power dissipation, variable adders, PDP; hybrid PTL/CMOS.

I. INTRODUCTION

Transmission of signals wirelessly. An antenna converts an In recent years, the increasing demand for high-speed and low power arithmetic units in floating point co-processors, image processing units and DSP chips has resulted in the development of high-speed adders, as addition is an obligatory and mandatory function in these units. A compact and a high-performance adder play an important role in most of the hardware circuits. Adders are used in microprocessor system based application for arithmetic addition and for computation in large electronics circuit. Less efficient and low power adders would lead to an increase in the total power dissipation in the circuit and delay as well, so processing in these devices is required to be accomplished by making use of low-power; area-efficient circuits processing at a higher speed. On the basis of requirements such as area, delay and power Consumption, different types of adder, such as ripple

Carry, the literature. Ripple carry adders shows the most compact design but slowest in speed, whereas carry look-ahead adder is the fastest one but it consumes more area. On the other hand, carry select adders act as a compromise between the two adders because it reduces the problem of carry propagation delay. However, the CSA generates partial sum and carry by using multiple pairs of Ripple Carry Adders (RCA) so it requires large area. CMOS circuits are most commonly used building blocks in digital integrated circuits.

II. ADDERS

One of the major concerns in VLSI design is power consumption. Power consumption has become an important factor due to continuous decline in size of CMOS circuits and increase in chip density and frequency at which circuits are operating. This paper presents a comparative analysis of various adders and proposed design of a new 32 bit carry select adder by sharing common Boolean logic term which shows

least power dissipation and PDP than other adders with less transistor count. This brief is structured as follows. Section II surveys various digital adders

A. Carry- Ripple Adder:

Carry-ripple adder (CRA) consists of cascaded "N" single-bit full-adders. Output carry of previous full adder becomes the carry input for the next full adder. Carry propagation delay exists between any two full adders in sequence For an N-bit full-adder as shown in Fig. 1, the critical path is equal to N-bit carry propagation path in the cascaded full-adders. As the value of N increases, the corresponding delay of carry-ripple adder will increase in a linear way. CRA has the slowest speed amongst all adders because of the large carry propagation delay but occupies the least area.
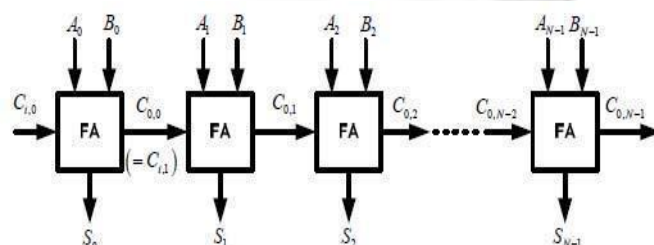

Fig. 1: N- bit CRA using N set single bit full Adders

B. Conventional Carry Select Adder

The block diagram of conventional carry select (CSA) adder is shown in Fig. 2. CSA uses CRA to generate sum and carry values using initial carry as 0 and 1 respectively, before the actually carry comes in. Upper CRA is fed with carry initial value as logic "0" while lower CRA is fed with carry initial value as logic "1". Multiplexer selects the result of carry "0" path if the previous carry is logic '0' or the result of carry "1" path if the previous carry is logic '1 i.e. actual carry is used to select the sum and carry using a multiplexer.
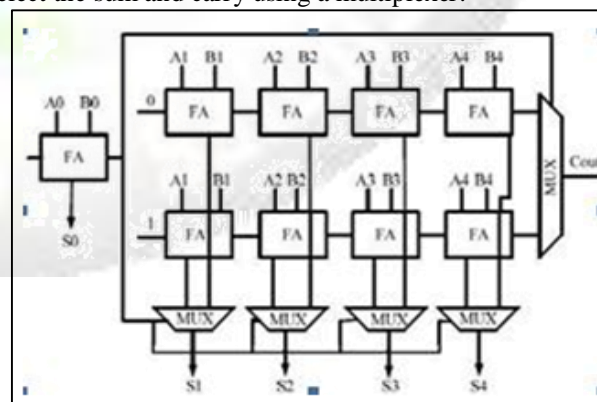

Fig. 2: Block diagram of conventional CSA

Each CRA pair in CSA can compute in parallel the value of sum before the previous stage carry comes. This reduces the critical path of an N bit adder. Delay in CSA is much lesser than CRA because the critical path in

case of conventional adder is N-bit carry propagation path and done sum generating stage while in case of CSA, the critical path is (N/L)-bit carry propagation path and L stage multiplexer with one sum generating stage in the N- bit CSA, where L is number of stages in CSA. Since L is much less than N and multiplexer delay is less than the delay in full adder, hence the delay in the CSA is much less than that in the CRA but there exists duplication of hardware in every stage which leads to an increase in the amount of power consumption and cost.

C. Improved Carry Select Adder

The truth table shown in Fig. 3 of a single-bit full-adder indicates that output sum (S0) is Ex-OR of inputs A and B when carry initial is logic "0" while output S0 is Ex-NOR of inputs A and B when carry initial is logic "1" as illustrate as two red circles in truth table. The improved CSA can be implemented by using this technique of sharing the common Boolean logic term in summation generation as shown in below.

Cin	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig. 3: Truth table for 1-bit full adder [1].

Hence we need to use Ex-OR gate and INV gate to generate the output sum signal pair. Sum output either the Ex-OR or the Ex-NOR could be selected using the multiplexer with select line as previous carry signal. The truth table also reveals that output carry (C0) is AND of A, B inputs when initial carry is logic "0" while C0 is OR of A, B when initial carry is logic "1".Same previous carry as select line to second multiplexer is used to select the carry output of the first stage which would act as select line of the multiplexers in the second stage. As both sum generation and carry generation is carried out in parallel therefore there exist some competitiveness in speed also the power consumption reduces as duplication of the hardware doesn't exist in improved CSA as in case of the conventional
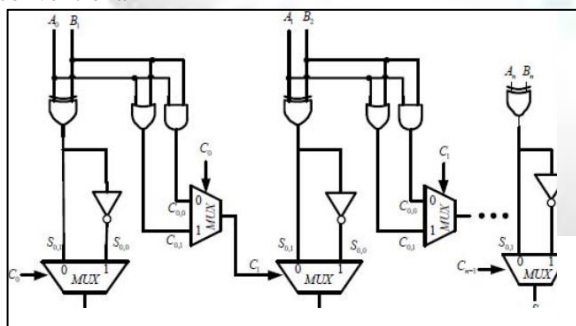

Fig. 4: Improved CSA

III. HYBRID PTL/CMOS LOGIC STYLE

PTL is considered to be better than static CMOS because it possesses the capability for carrying out a logic function with less number of transistor counts, less delay and

less power dissipation [8], [9], [10], and [11]. In order to obtain full swing output, at PTL output gate, restoring logic is required consequently power dissipation of PTL circuits would increase along with slowing down the circuit with these level- restoring logics.

PTL based multiplexer structure and XOR have less power (which includes dynamic power as well as static leakage power), power Delay product and less area. For NAND and NOR intensive circuit [10], PTL doesn't give good results while static CMOS do. Hence PTL is not considered better than CMOS for i implementations of all types of logic structures.

Since CMOS and PTL implementation have their respective advantages and disadvantages in terms of Power Dissipation, Power Delay product and Area, HYBRID PTL/CMOS could result in better implementation n with respect to area, power and delay. HYBRID PTL/CMOS implantation of logic structure makes use of a Hybrid combination of CMOS and PTL logic style. Hybrid combination implements advantages of CMOS as well as PTL logic styles. Binary decision diagrams (BDD) [10], [11] can be used to represents a logic function in HYBRID PTL/CMOS logic style.

IV. PROPOSED CARRY SELECT ADDER

Implementation of proposed carry select adder has been done using HYBRID PTL/CMOS logic style with the help of BDD. The schematic diagram of proposed CSA is shown in Fig. 5. In the proposed design, improved CSA design is implemented using HYBRID PTL/CMOS logic style, where bitonic circuits are implemented using PTL and monotonic circuits is implemented using CMOS logic style. In proposed CSA design, each unit represents 4 bit full adder. An instance of 4 bit full adder has been replicated 8 times to form 32 bit Proposed CSA. Carry out of each stage is input to the next stage carry input. It encapsulates the advantages of both PTL and CMOS logic style.

V. SIMULATION RESULTS

Implementation of 32 bit Carry Select Adder using Hybrid PTL/CMOS logic has been done on Predictive Model Beta Version 90nm CMOS technology. Simulation results of Power Dissipation and PDP are shown in Table I. It has been found that the area, power dissipation, power delay product of the proposed 32 bit carry select adder using Hybrid PTL/CMOS logic style is less than that of the improved CSA, conventional CSA, and conventional CRA. Analysis shows that it results in 48 to 52 percent less power dissipation and 40 % less PDP when implementation is done using Hybrid PTL/CMOS logic style in comparison to improved design at a 1.5 volts operating voltage. Fig. 6 depicts power dissipation comparison graph of CRA, Conventional CSA, and Improved CSA over different values of supply voltages (Vdd). Here Fig. 7 depicts power delay product comparison graph for all the four adders.
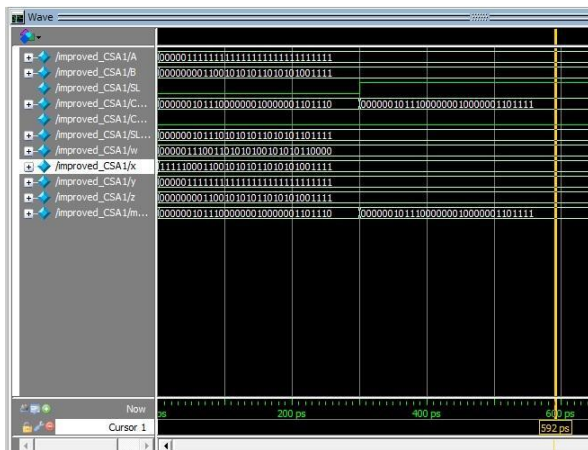
Fig. 5: Simulation for Hybrid PTL/CMOS Top level Module

VI. CONCLUSION

In VLSI design, power and area are the constituent factors which limit the performance of any circuit. High Performance and power efficient circuits can be designed using Hybrid PTL/CMOS logic style. Hence 32 bit CSA using Hybrid PTL/CMOS logic style has been proposed. It has been found that the transistor count, power dissipation of the improved adder using Hybrid PTL/CMOS logic style is less than that of other conventional designs .The comparisons of adder design are based upon Predictive Model Beta Version 90nm CMOS technology in tanner EDA tool.

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