A Study of Multigate Transistor & Radiation Effects On Semiconductor Devices

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Abstract— *This paper presents the radiation effect of Multigate transistors. MOSFET is the workhorse of the micro electronics industry. As transistors are being shrunk in size, their switching behavior becomes even poorer. Such 'multigate' architectures will allow a further shrinking in size without downgrading transistor performance. In this review we discuss the radiation damage mechanism. The basic mechanisms of space radiation effects on microelectronics. The naturally occurring space radiation environment produces transient and permanent changes in the electrical properties of solid-state devices and integrated circuits.*

Keywords— Multigate Architecture, Radiation effects in semiconductor device,

I. INTRODUCTION

MOSFETs are the building blocks of microprocessors, memory chips and telecommunications microcircuits. A modern microprocessor can contain more than 2 billion MOSFETs, and a 32-gigabyte memory card weighing only 0.5 g contains a staggering 256 billion transistors, which is comparable to the number of stars in the Milky Way. MOSFETs are mainly used as switches in logic microcircuits, although they can fulfill other purposes. In Multigate architecture, replacing silicon dioxide as a gate insulator with other metallic oxides that have a higher dielectric constant .

MOSFET consists of two n-type semiconductor regions called the source and the drain, which are separated by a region of p-type semiconductor called the substrate. This description is for an n-channel MOSFET, or NMOS device. A p-type MOSFET, or PMOS device, would have the opposite doping in the source, drain and substrate regions. Typically, the semiconductor is silicon, although other semiconductor materials, with faster charge carriers, are being considered by the microelectronics industry.A thin layer of insulating material such as silicon dioxide covers the region between the source and the drain, and this layer is topped by a metal electrode called the gate. A large enough positive voltage is applied to the gate, then electrons 'spill out' of the n-type semiconductor source and drain regions, forming an electron-rich layer, called the channel, underneath the gate oxide[1].

As transistors are being shrunk in size, their switching behavior becomes even poorer. One solution is to abandon the planar configuration and to design a gate electrode that is wrapped around several sides of the conducting channel, improving electrostatic control over the channel. Such 'multigate' architectures will allow a further shrinking in size without downgrading transistor performance.

II. MULTIGATE ARCHITECTURE

For more than four decades, transistors have been shrinking exponentially in size, and therefore the number of transistors in a single microelectronic chip has been increasing exponentially. Such an increase in packing density was made possible by continually shrinking the metal–oxide–semiconductor field-effect transistor (MOSFET)[1]. Recently,however, a new generation of MOSFETs, called multigate transistors, has emerged, and this multigate geometry will allow the continuing enhancement of computer performance into the next decade [1].

In a classical 'bulk' MOSFET, the gate electrode is situated on top of an insulator (an oxide) that covers the channel region of the device between the source and the drain. In such a configuration, the device is planar and essentially two dimensional. Electrostatic control of the channel by the gate is achieved through capacitive coupling between the gate and the channel region, through the gate insulator [1].

The scaling laws require a reduction in the depth of the source and drain regions by the same scaling factor as the gate-length reduction. This reduces short-channel effects by rendering less effective the control of the channel region by the source and the drain. Decreasing the thickness of the gate oxide yields a similar result, by improving the capacitive coupling between the gate and the channel.

In addition, replacing silicon dioxide as a gate insulator with other metallic oxides that have a higher dielectric constant can significantly enhance the gate capacitance, which, in turn, yields a higher current. Hafnium oxide and lanthanum lutetium oxide have dielectric constants that are fivefold and eightfold higher than that of silicon dioxide, respectively [1][2]. Using these materials results in much greater control of the channel by the gate voltage and thus in a reduction in short-channel effects.

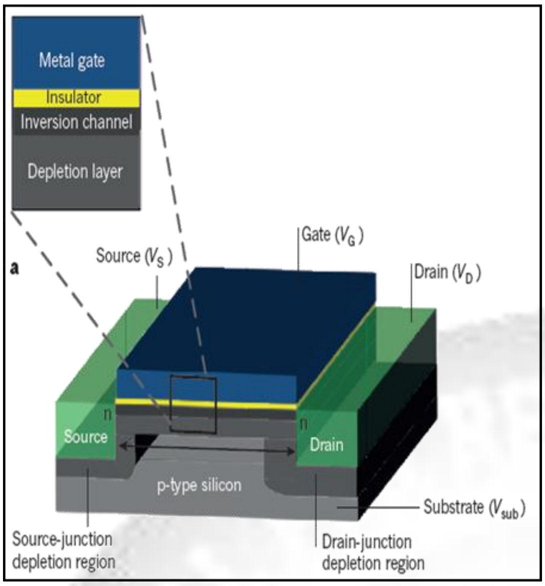

Fig. 1: A schematic view of a classical bulk n-channel MOSFET [1]

Multigate MOSFETs take advantage of a third dimension to counteract short-channel effects. The term multigate is perhaps not the most appropriate one, as these devices have gate electrode. It simply means that the electrode is wrapped around several sides of the channel region.

III. RADIATION EFFECTS IN SEMICONDUCTOR DEVICES

Semiconductor devices planned for use in outer space have unique reliability challenges because of the high radiation levels present outside of Earth's atmosphere [5]. If not properly designed, semiconductor devices exposed to radiation can have significant degradation and high error rates, potentially leading to costly system failures [5]. Therefore, understanding how devices are affected by radiation, and how they can be designed to avoid these issues is of utmost importance.

Here, a review of the effects of radiation on semiconductor devices will be presented, which can be broken down into two categories, total ionizing dose effects and displacement damage effects, discussed in more detail in the subsequent [5].

A. Total Ionizing Dose Effects:

Total ionizing dose (TID) effects refer to the degradation of device performance due to the cumulative effects of ionizing radiation exposure. When an energetic particle passes through a semiconductor, the energy is lost to Coulomb scattering within the target material, ionizing atoms and creating electron-hole pairs (EHPs) along the particle track [6].

The number of EHPs generated by a particle is related to the energy absorbed by the target, determined by both the particle type and energy, and the target material density. The energy absorbed by the target material from radiation is usually presented in terms of rads, with 1 rad=0.01 J/kg. Since the radiation absorbed is dependent on the material [5][6].

Primarily, TID effects from radiation are due to generated electrons and holes that become trapped within insulators. They in turn electrostatically couple to the semiconductor and alter device behavior. As such, MOSFETs which contain different insulating layers that is in contact with sensitive device regions are especially sensitive to TID radiation.[7] Within a MOSFET, three insulating layers that tend to cause TID device degradation are the gate oxide.

The TID effects in the gate oxide of a MOSFET can be explained using a diagram of a metal-oxide-semiconductor (MOS) capacitor, drawn in Fig 3[5].

The radiation creates EHPs in the silicon dioxide (SiO2) gate oxide, with some fraction recombining and some splitting into free electrons and holes.The fraction of EHPs that become free electrons and holes is increased in the presence of an electrical field, which can occur across the gate oxide of a MOS capacitorwhen the gate is biased [5].

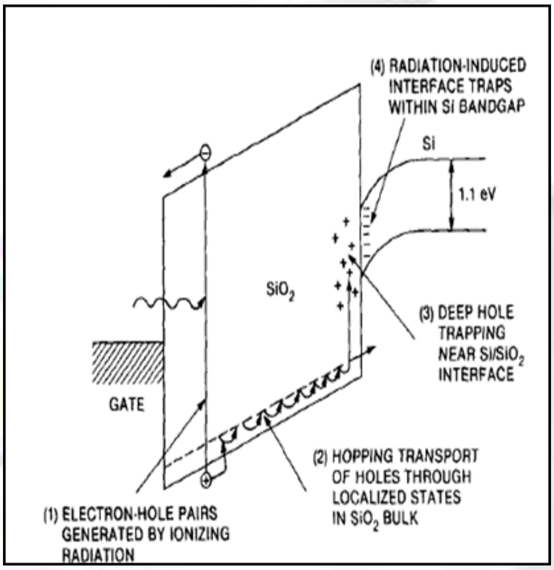

Fig. 3:

Fig. 3.Diagram of metal oxide semiconductor system exposed to ionizing radiation. EHPs are generated within the gate oxide and electrons quickly travel out, while holes remain trapped. Some holes remain trapped in deep trap states and act as fixed trap charge, while others drift to the insulator-semiconductor interface and form interface trap states[5].

Since an increase in the yield of free electrons and holes during irradiation can affect the radiation response, often devices are held at a variety of different bias configurations during radiation exposure to simulate the worst case effects from electron and hole generation. Although both free electrons and holes are created, in SiO2 electrons have a higher mobility relative to holes and can escape from the gate oxide, whereas holes tend to remain.[5] The holes within the gate oxide can be drawn towards the silicon channel by the electric field from the gate, shown in Fig. 3 but they often become trapped within deep trap states and act as fixed positive charge, screening the electric field coming from the gate and creating negative threshold voltage shifts in MOSFETs.[7],[5] The holes not trapped in deep states within the gate oxide can move to the Si-SiO2 interface and create interface trap states that increase the subthreshold slope in MOSFETs and alter the threshold voltage further, degrading device performance[7].

More recently, TID effects on gate oxides has lessened considerably due to gate oxide scaling, which has resulted in gate oxide thicknesses of only a few nanometers or less[7]

B. Displacement Damage Effects:

Displacement damage (DD) refers to the damage done to the crystal lattice by incident radiation [5]. Radiation particles can interact with the valence electrons, losing energy through ionization, discussed previously, or through non-ionizing energy loss (NIEL) mechanisms such as collisions with lattice atoms.[6] If enough energy is imparted to the lattice atom, it can knock anatom from its lattice position, creating defects in the crystal. These defect form band gap states that degrade the electrical performance of devices [5]

For atoms to be displaced from lattice sites a minimum energy is necessary, referred to as the displacement threshold energy which is material specific. Displacement threshold energies tend to range from 5-30eV for common semiconductors, with silicon having a value of 21eV. [6]

The lattice atom that is displaced is referred to as the primary knock-on atom (PKA), and may absorb more energy than the displacement threshold energy[5]. It can move through the crystal as an energetic ion that can cause secondary displacements, referred to as a defect cascade[5].

The incident particle energy also plays a role in the displacement damage that occurs in a material. This is illustrated in Fig. 4 which plots the displacement damage processes as a function of incident proton energy in silicon.[5] For proton energies below 6-10 MeV, single point

defects tend to be produced, with the recoil energy of the PKA low enough that secondary displacements are unlikely. As the proton energy increases above 6-10MeV, the likelihood of

secondary displacements increases.

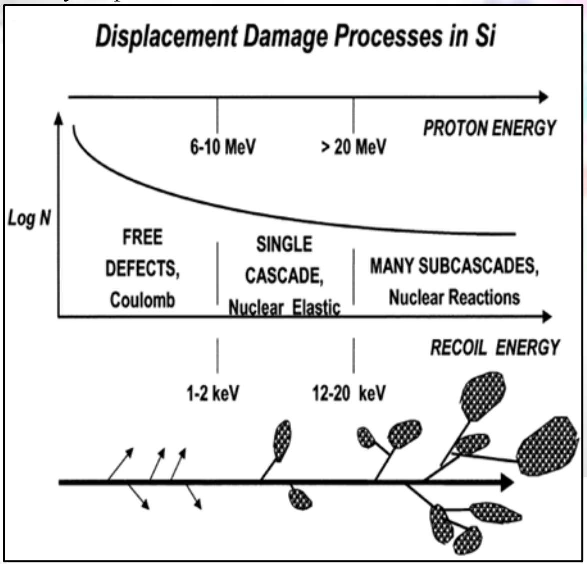

Fig. 4:

Fig 4. An illustration of the displacement damage processes using proton radiation insilicon. As the proton energy increases, damage increases from single point defects to larger damage clusters from secondary collisions to a full damage cascade with many large damage clusters[5].

The primary effect of the lattice damage on the electronic properties of semiconductor devices comes from the creation of band gap states[5].

IV. Conclusion

In this paper we concluded that a radiation effect in multigate transistors has been presented. Specially, TID form the built up of charge within insulating layer of a device and displacement damage and defects within the semiconductor lattice.

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