A Survey of Design of RBS for Low Power VLSI

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Abstract— *with the rapid growth of the portable electronic equipment, wearable computers, laptops, cell phones etc. the demand of the low power very large scale integration (VLSI) is dynamically increasing. The power consumption is one of the top most crucial limiting factors of the concern for the designing of the low power electronic circuits for the today's & even before this era [1]. The numbers of scientists/ researchers are struggling for overcoming such a limiting factor/ obstacle and proposing different ideas and designing methods from the logical level (Gate Level) to circuitry level (Physical level) and above for the very large scale integration Even after of such a struggle, there is no any universal method to design to avoid tradeoff between delay, power consumption and complexity of the circuit. Still, the designer is required to opt appropriate technology for satisfying product need and applications [2].*

Keywords— VLSI, Gate Level, Physical Level

I. INTRODUCTION

For the designing of the digital hardware, the logical architecture is the most commonly method of defining the structure and relationship of the subcomponents of a system. For a hardware implementation, the numbers of designers in the industries works on the different level of the designing. These levels of design describe the concepts of implementation, primarily logical conceptual system. There are many levels of detail are required to completely specify a given implementation. John Von Neumann was the first person who describes the architecture definition and the organization of logical elements in 1945[3][4]. The different level for designing of digital hardware which has to follows by the hardware designers is briefing below and shown in fig 1.1 [2].The first level is algorithm and this is most one process of design which is "a set of rules that defines a sequence of operations." Then high level language is the further process in which the designer interprets an algorithmic description of a desired behavior and creates hardware that implements that behavior.Machine code is a system of impartibly instructions and each instruction performs a very specific task, typically either an operation on a unit of data. Computer architecture is the practical art of defining the structure and relationship of the subcomponents of a computer. Logic Implementation is the design of blocks defined in the micro architecture at (primarily) the register-transfer level and logic gate level. In the Physical Implementation level, the different circuit components of the circuit are placed in a chip floor plan or on a board and the wires connecting them are routed

II. BACKGROUND HISTORY

In this section, I briefly summarize some of the history of reversible computing research. There are numbers of the designing approach at the logical level for reducing the power consumption in the systems. Few of them are main concerning towards the complexity of the circuits, cost and delay etc. But the reversible logics or reversible computing is one of the strongest and the effective way to reduce the power consumption or heat loss. As due to quantum computing which is also a emerging technology, reversible logics has the greatest applications in such a field specially[13][14]. So, reversible logics are one of the effective solutions of the heat loss at the logical level. Historically, The study of thermodynamically and logically reversible computational processes has been motivated by concerns in fundamental physics where it is required to understanding that the means of disposal of unwanted information can be important when considering the thermo dynamics of a system. [2]. John Von Neumann was the first person who made the first connection between computation and fundamental thermodynamics. In 1949, he performed a calculation, that is, per elementary decision of a two-way alternative and per elementary transmittal of 1 unit of information at the University of Illinois, Unfortunately, there is apparently no existing complete record of this lecture, or of any corresponding written analysis by von Neumann, so it is difficult to determine exactly how he explained this analysis, how seriously he to it [2] [15]. But in 1961, Rolf Landauer in ref.[1] was the person who made a connection between computation and fundamental thermodynamics and stated that the system designed by conventional approach or in irreversible manner dissipated heat of equal to KTln2 on every bit computation. Where K is the Boltzmann's constant equal to 1.3806505 × 10-23 m2kg2k-1 and T is the temp. at which the logical computation is performed. In 1973, Charles Bennet [5] was one of the scientists which showed that the amount of energy which was predicted by the Landauer in 1961 can be directly correlated to the information lost. i.e. according the Bennet, on every bit of information loss there is a heat loss of KTln 2. Charles Bennett [5] also discovered that the reversibly-recorded history of an irreversible computation could also be cleared in a logically reversible way, leaving only the input and the desired computational output in memory. This theory of the reversible computing has been accepted yet and now the concerning was on the question how we design the reversible systems. In 1980, Toffoli [16] proposed a reversible gate named toffoli gate, a basic gate to realize the numbers of Boolean expressions. The quantum cost of this gate is 5. Quantum cost is one of the parameter in the designing of the reversible logics which keeps being low as much as possible [17]. This gate was generally used in the starting of the designing approach but now due to more effective reversible gates this gate is used in the less quantity. Numbers of researchers proposed their reversible gates modules for the designing of the reversible logics with their quantum representation. Few of them are

Reversible Gate	Ref. No.	Researcher Name
Toffoli	16	T. Toffoli

Feynman Gate	4	Feynman
Fredkin gate	8	Fredkin
TSG gate	52	Himanshu Thapliyal
PG	14	A. Peres
NFT	31	M. Haghparast et al.
MG	6	Abu Sadat el Al

Table 1: Brief of reversible gates in the Literature

There are more and many researchers who designs the numbers of the reversible logics structure like Adder, Subtractor, Division hardware, Multiplexer, Register, Counter etc [4]. But these designs are used for only a specific purpose not for the universal purpose. The Barrel shifter is an integral component of many computing systems due to its useful property that it can shift and rotate multiple bits in a single cycle. So, this dissertation work is directed towards such a design

A. Design of RBS at The Logical Level

There are number of reversible logic structure for different functions for example Adder , Subtractor, Half adder ,Full adder etc .But in this dissertation I focusing on the reversible structure of barrel shifter having their own specific importance in many key computer operations from adder generation to arithmetic operations and in DSPs where multiple shifts are required to do computations such as FFT, circular convolution etc. Shifting a single data bit one field at a time can be a slow process, So Barrel shifter are used to produce multiple shifts in only one clock cycle. A Barrel shifter is combinational logic circuit that can shift or rotate a data word by any number of bits in single operation .In the existing literature there exist designs of RBS that can only perform left rotation operation. The proposed architecture was unidirectional in nature. In this dissertation I proposed a bidirectional arithmetic and logical barrel shifter that can perform logical right shifting , arithmetical right shifting, logical left shifting, arithmetical left shifting. The reversible fredkin and Feynman gates are basic building blocks of design. In this am going to propose an optimise structure of bidirectional RBS by using the reversible gates.

1) Reversible Logic Gates

The elementary building block of a digital circuit is called logic gate. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions low (0) or high (1), represented by different voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state is approximately zero volts (0 V), while the high state is approximately five volts positive (+5 V).Reversible gates are the special gates which are having bijective function between its input function and output functions. An N×N reversible gate can be represented as [4].

$$IV = (I1,I2,I3,\ldots,\ldots,\ldots,IN)$$
$$OV = (O1,O2,O3,\ldots,\ldots,\ldots,ON)$$

Where Iv = input vectors ,Ov= output vectors

When a device can actually run backwards then it is called physically reversible and the second law of thermodynamics guarantees that it dissipates no heat.

2) Reversible Barrel Shifter

A barrel shifter is a n-inputs and n-outputs combinational logic circuit in which k select lines controls the bit shift operation. Barrel shifter can be unidirectional allowing data to be shifted only to left (or right), or bi-directional which provides data to be rotated or shifted in both the directions. A barrel shifter having n inputs and k select lines is called (n,k) barrel shifter. Among the different designs of barrel shifter, the logarithmic barrel shifter is most widely used because of its simple design, less area and the elimination of the decoder circuitry. The conventional irreversible design of a logarithmic barrel shifter is shown in Fig.1.1. A n-bit Logarithmic Barrel Shifter contains log2(n) stage where the ith stage either shifts over 2i bits or leaves the data unchanged. Each stage of a logarithmic barrel shifter is controlled by a control bit. If the control bit is set to one then the input data will be shifted in the associated stage else it remains unchanged. The proposed work presents the design methodologies for RBS that can perform six operations: logical right shift, arithmetic right shift, right rotate, logical left shift, arithmetic left shift and left rotate. For illustration, all of these operation are as shown in Table 1.1 for an 8 bit logarithmic barrel shifter where the 8 bit input data is denoted as i7, i6, i5,i4, i3, i2, i1, i0 here i7 is the sign bit, and the shift or rotate operation is performed by 3 bits, and X denotes the shifted result.

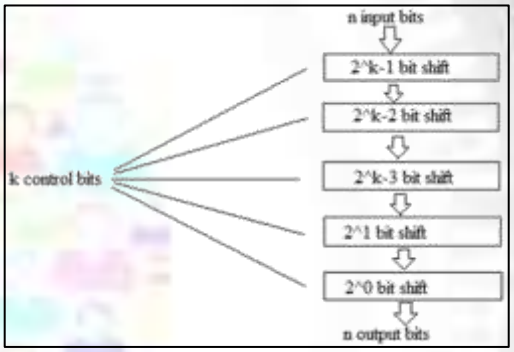

Fig. 1: Structure of (n,k) logarithmic barrel shifter

Operation Performed	X(Final Output*)
Logical Right Shift	$000i_7i_6i_5i_4i_3$
Arithmetic Right Shift	$i_7i_7i_7i_7i_6i_5i_4i_3$
Right rotation	$i_2i_1i_0i_7i_6i_5i_4i_3$
Logical Left Shift	$i_4i_3i_2i_1i_0000$
Arithmetic Left Shift	$i_7i_3i_2i_1i_0000$
Left Rotation	$i_4i_3i_2i_1i_0i_7i_6i_5$
*The input data is $i_7i_6i_5i_4i_3i_2i_1i_0$ here i_7 is the sign bit	

Table 2: Operations on an 8 bit barrel shifter with 3 bit shift value

All operation that can be performed by a logarithmic barrel shifter as shown in Table 2 are as follows:

a) Logical Right Shift

As shown in Table 2 a 3-bit logical right shift operation right shifts the input data by 3 bits and sets the leftmost 3-bits to zero thus the output will be 000i7i6i5i4i3

b) Arithmetic Right Shift

A 3-bit arithmetic right shift operation right shifts the input data bit by 3-bits and sets the leftmost 3-bits to the sign bit (i7) thus the output will be i7i7i7i7i6i5i4i3.

c) Right Rotation

A 3-bit right rotation operation performs a right shift operation on input data by 3-bits. Further, the leftmost 3-bits are set to the rightmost 3-bits of the original input data. Thus, as shown in the Table 2 the final output after the right rotation operation will be i2i1i0i7i6i5i4i3 as the input data

i7i6i5i4i3i2i1i0 is shifted 3 times to the right and the 3 leftmost bits (i7i6i5) are set to the 3 rightmost bits (i2i1i0) of the original data.

d) Logical Left Shift

A 3-bit logical left shift operation left shifts the input data by 3-bits and sets the rightmost 3-bits to zero thus the final output will be i4i3i2i1i0000.

e) Arithmetic Left Shift

In the arithmetic left shift operation the sign bit of the input data remains intact and the remaining bits are logically left shifted by 3-bits. Thus as shown in the Table 1.1 the output will be i7i3i2i1i0000 as the input data i7i6i5i4i3i2i1i0 is logically left shifted by 3-bits and the sign bit (i7) remains intact.

f) Left Rotation

A 3-bit left rotation operation performs a left shift operation on input data by 3-bits. Further the rightmost 3-bits are set to the leftmost 3-bits of the original input data. Thus as shown in the Table 1.1 the final output after the left rotation operation will be i4i3i2i1i0i7i6i5 as the input data i7i6i5i4i3i2i1i0 is shifted 3 times to the left and the 3 rightmost bits (i2i1i0) are set to the 3 leftmost bits (i7i6i5) of the original data.

B. Reversible Computing

Whenever a computing Engine performs a logical operation, there are number of unwanted bits after operation which are thrown away with the sudden change of voltage from positive to negative and dissipated as heat. Even ever shocking that, why the computing machine becomes so hot on use. The performance of the system is increases by either reducing the supply or by providing the cooling effect by fan [15]. But this is the limiting factor that, the computing engine or systems throw away unwanted bits after operation in the form of heat. So, Reversible logics are one of the better alternate to reduce or overcome such a power dissipation factor. Actually reversible logics are the adiabatic systems that recycle their energy and emit very little heat or ideally zero heat [24]. In case of the reversible logics, rather than the changing voltage to new levels, the reversible circuit elements will gradually move charges from one junction to next junction [25].

1) The Concept

The basic concept of the use of Reversibility was come from the mechanical engineering branch thermodynamics which taught us the benefits of the reversible systems over irreversible system [3]. In mechanical engineering, whenever a mechanical engineer designs a heat engine, he takes Carnot cycle as a reference. His main concern is to make the engine as much as highly efficient. According to the second law of thermodynamics, The entropy of the engine never be decreased and the efficiency of the heat engine is measures by how much incoming heat energy Q producing the work done W. an amount Q of high-temperature heat energy, and produces an amount W of work. The heat engine's efficiency is thus ηh.e. = W/Q (Dimensionless) [10]. ηh.e < 1 because of the conservation of energy.

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2) Development in RBS

There are numbers of the reversible logic structure for the different function but in this dissertation I focus on the Barrel shifter which has their own specific importance in embedded digital signal processors and general purpose processors to manipulate data. The main objective of the upcoming designs is to increase the performance without proportional increase in power consumption. In this regard reversible logic has become most popular technology in the field of low power computing, optical computing, quantum computing and other computing technologies. Rotating and data shifting are required in many operations such as logical and arithmetic operations, indexing and address decoding etc. Hence barrel shifters which can shift and rotate multiple bits in a single cycle have become a common choice of design for high speed applications. In [4], an irreversible shifter has been described. This shifter shown in Figure 1.2 consists of several transmission paths which are built from simple n-type transistors. The control lines operate vertically, the input lines rise diagonally and the output lines run horizontally. At a time exactly one control line is set which turns on all the switches in a single column. The length of the shifting is determined by the position of the selected column. Thus all the inputs are shunted to the output lines. This shifter is very simple in design and transmission delay is minimal while the circuit requires large area

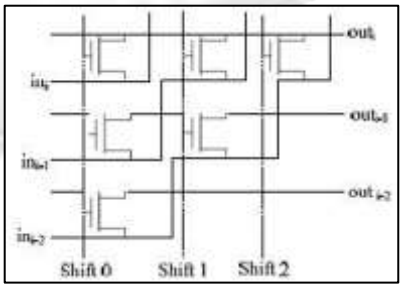

Fig. 2: Barrel Shifter

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