Design of Reversible Barrel Shift Register

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Abstract— *the power consumption is one of the top most critical limiting factors of the concern for the designing of the low power electronic circuits. This concept could be understand as the irreversible system which are designed by the traditional approach dissipates KTln2 of heat/ energy on every bit of computation as predicted by Rolf Landauer in1961[1]. Where K is the Boltzmann's constant equal to 1.3806505 × 10-23 m2kg2k-1(J/K) and T is the temp. at which the logical computation is performed. This dissipated energy is directly correlated the number of lost bits [5]. Reversible logics use the charge recovery process to save energy. These are the logic which does not loose information [6]. The reversible circuits are designed by the special logical gates called reversible gates. Reversible logic structure posses the property of one to one mapping between the inputs and output state [6-8]. There is no any universal method to design to avoid tradeoff between delay, power consumption and complexity of the circuit. Still, the designer is required to opt appropriate technology for satisfying product need. Reversible logics are the logic which does not dissipate the power, uses this concept in designing of digital VLSI system. In reversible logic gates there is a unique one-to-one mapping between the inputs and outputs. To generate an useful gate function the reversible gates require some constant ancillary inputs called ancilla inputs. The number of ancilla inputs, number of garbage outputs and quantum cost plays an important role in the evaluation of reversible circuits. Thus minimizing these parameters are important for designing an efficient reversible circuit. Barrel shifter is an integral component of many computing systems due to its useful property that it can shift and rotate multiple bits in a single cycle. The main contribution of this thesis is a set of design methodologies for the reversible realization of RBS where the designs are based on the Fredkin gate and the Feynman gate. The Fredkin gate can implement the 2:1 MUX with minimum quantum cost, minimum number of ancilla inputs and minimum number of garbage outputs and the Feynman gate can be used so as to avoid the fanout, as fanout is not allowed in reversible logic. The design methodologies considered in this work targets 1.) Reversible logical right shifter (RLRS), 2.) Reversible universal right shifter (RURS) that supports logical right shift, arithmetic right shift and the right rotate, 3.) Reversible bidirectional logical shifter (RBLS), 4.) Reversible bidirectional arithmetic and logical shifter (RBALS), 5) Reversible universal bidirectional shifter (RUBS) that supports bidirectional logical and arithmetic shift and rotate operations.*

Keywords— VLSI, Reversible

I. INTRODUCTION

A. *Reversible Logic*

The RTL views, the simulation results and the quantized results of the proposed RBS (RBS). The simulation results shows the verification of the design by using the XILINX 8.2ISE software and the quantized results shows the calculative results based on the different parameters calculation. Register-transfer level (RTL) is a design abstraction which model the digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals.

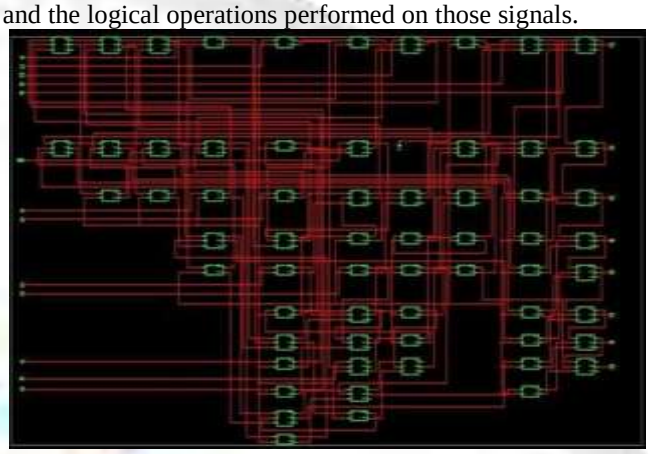

Fig. 1: RTL view of (8, 3) RLRS

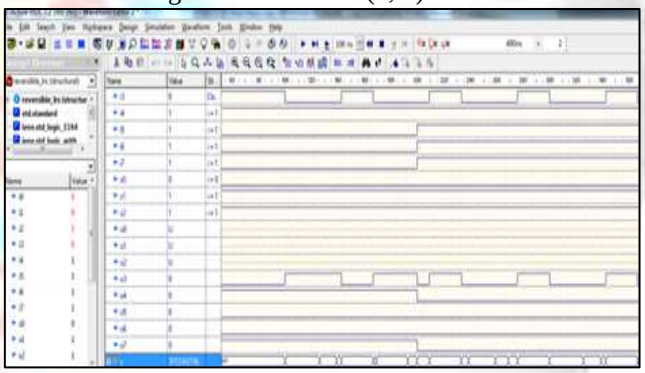

Fig. 2: Simulation Result for RLRS

B. *RTL of (8, 3) RURS*

The RTL view of Proposed RURS is shown in the fig.3.

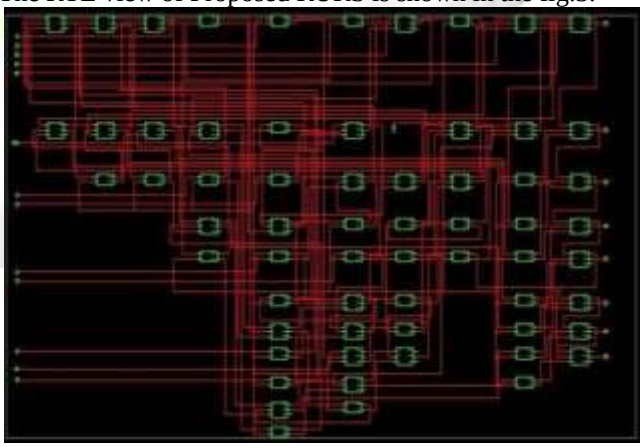

Fig. 2: RTL view of (8, 3) RURS

C. *Simulation Result for RURS*

The simulation result for (8,3) RURS is shown in the fig.4.

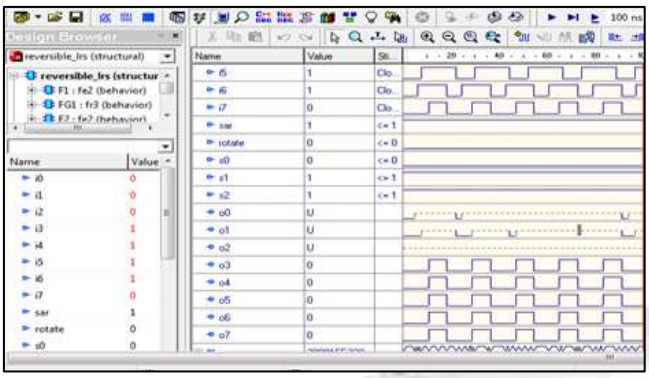

Fig. 4: Simulation result of RURS

D. Simulation Result for RBALS

The circuit is capable of logical shifting the input data in both the left and right directions.

E. RTL of (8, 3) RBALS

The RTL view of Proposed RBALS is shown in the fig 5.

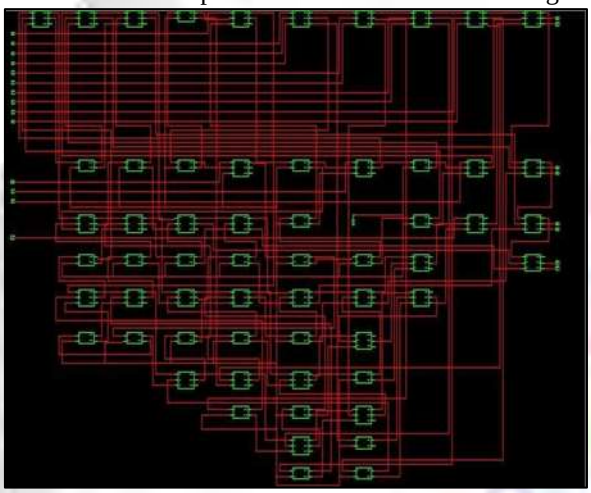

Fig.5 RTL view of (8,3) RBALS

F. Simulation Result for RBALS

The simulation result for (8, 3) RBALS is shown in the fig.6.

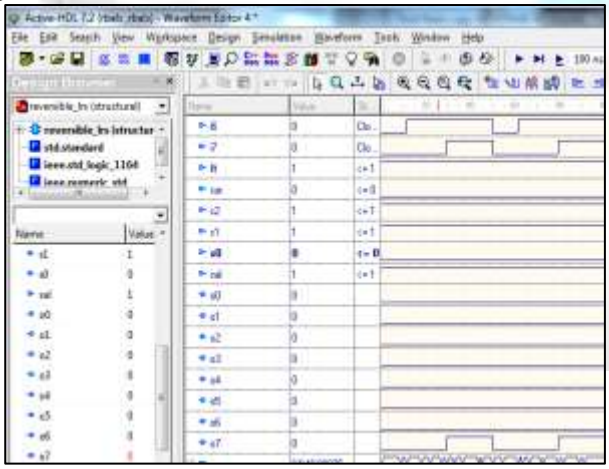

Fig. 6: Simulation result of RBALS

II. CONCLUSION

A hardware designer goes through the different levels for the design. In this dissertation, a new approach i.e. the reversible logical approach has been proposed for the design of the electronic system at the logical level.

A. Garbage Outputs

In this RBS implementation, we can see that there are two outputs of the Feynman gate corresponding to the inputs. In this the complementary function and the copying function is generated and they further utilized in the circuit. Thus, we can say that the garbage output is zero for this implementation.

B. Constant Inputs

The number of inputs that are kept constant (0 or 1) for synthesis the given functions and in all the reversible gates used constant inputs (0 or 1) for producing the different outputs.

C. Quantum Cost

As we have used Feynman gate whose quantum cost is 1 and Frdekin gate whose quantum cost is 5. So, if there are n number of fredkin gate then quantum cost is 5n. So, our proposed structure for RBS is efficient than existing one because of less quantum cost and total logical calculations.
In this paper the basic introduction with the designing procedure of the electronic system is extrapolated by explaining each step. The complete literature of the reversible logic and the barrel shifter is also describes in the dissertation by proper explanation. The different reversible gates like Feynman and Fredkin gate is shown with the proper relation of inputs and outputs.

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