Low Power and High Speed FIR Filter based on a New Window Technique for System on Chip

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Abstract— *In this paper, we have described a new digital low pass FIR filter implemented using a new window function. We have demonstrated the analysis of performance of different window functions used to design and implement the digital FIR filter on SoC. The different window techniques used are Rectangular, Hanning, Hamming, Bartlett and Kaiser Window Function, with sampling frequency 48 KHz and with cut off frequency 10.8 KHz. We do the comparison for these for different order i.e. 20, 40, 60 upto 120. It is shown that filter design by using Kaiser Window function is best in terms of minimum power consumption whereas Hanning window function in terms of minimum time required for simulation. Thus authors have combined both window function and formulated a new adjustable window function, that over comes the tradeoff between Kaiser and Hanning for power and delay. The new proposed window function gives intermediate results when compared with other two. We have concluded the calculated parameters i.e. Power Consumption (Static and Dynamic), and Delay for different window function along with the proposed window function. Based on the coefficients, FIR filter is being modeled in Matlab 2013A using FDA tool and programmed in HDL coder using and finally synthesized and simulated on Xilinx design suite 14.4 ISE for time analysis and Xilinx Plan Ahead for power analysis.*

Keywords— FIR, IIR, HDL, Verilog, FPGA, FDA

I. INTRODUCTION

The developments in electronic technology, growth in mobile computing and portable multimedia applications are taking place at a tremendous speed. The battery lifetime of portable electronics has become a major design concern as more functionality is incorporated into these devices. Since many telephony and data communications applications have been moving to digital, and with the advancement in VLSI technology, the need of low power circuits for digital filtering methods continues to grow[10]. This resulted in increased demand for Digital Signal Processing (DSP) System. One of the most widely used operations performed in DSP is digital filtering. Other than this, DSP is used in numerous applications such as video compression, digital set-top box, multimedia and wireless communications, speech processing, transmission systems, radar imaging, global positioning systems, and biomedical signal processing [11].

An operation of digital filter design is calculation of filter transfer function coefficients that decide the response of the filter. Typical filter applications include signal preconditioning, band selection, and low/high pass filtering. Digital Filters are categorized as Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) Filter. Reason for choosing FIR filter over IIR is that FIR filter has strictly linear phase, non-recursive structure, arbitrary amplitude-frequency characteristic, high stability and real-time stable signal processing requirements etc [6].

Real time high speed realization of FIR filters with less power consumption has become much more demanding and is a challenging task. Since the complexity of implementation grows with the filter order and the precision of computation, several attempts have, therefore, been made to develop dedicated and reconfigurable architectures for realization of FIR filters in Application Specific Integrated Circuits (ASIC) and Field- Programmable Gate Arrays (FPGA) platforms. Based on the literature survey [2-6], we can conclude that:

- Either it takes into consideration one particular filter design technique
- Or it takes into consideration filter order
- Or a particular family of FPGA
- Or it takes into consideration either power, resource or delay

This paper provides an extended version of the conference paper presented.[1] The paper has been extended to provide: (i) extended background information, (ii) Experimental methodology details (iii) New window function (iv) Comparison of results (v) Conclusion.

The rest of the paper is organized as follows: Section II describes the basic principle and structure for FIR filter. Section III presents the window function method for FIR filter design and the classic window shapes. Section IV describes the design specification of filter. Section V presents the proposed objective. Section VI introduces the experimental methodology used. Analysis of parameters for exciting window functions are presented in section VII. Section VIII describes the power reduction using adjustable window function. Finally conclusions and future scope are presented in Sections X.

II. BASIC PRINCIPLE AND STRUCTURE OF FIR FILTER

Linear Time Invariant Finite impulse response filters constitute the backbone of DSP systems and are the most common digital filter. Signal separation and signal restoration are the two uses of filters. Signal restoration is used when the signal has been distorted in some way. While when the signal has been contaminated with noise or other signals, signal separation is needed. The direct form realization structure of FIR filter can be described by simple convolution operation as described by equation(1), where x is input signal, y is convolved output and h is filter impulse response.

$$y(n) = \sum_{k=0}^{N-1}[h(k)*x(n-k)] \quad (1)$$

The desired frequency response Hd ($e^{j\omega}$) of any digital filter is periodic in frequency and can be expanded in a Fourier series, using the following relation [9]:

$$Hd(e^{j\omega}) = \sum^{\infty} [hd(n) * e^{-j\omega n})]$$

Where $hd(n) = 1/2\pi \int^{2\pi} Hd(e^{j\omega}) * e^{j\omega n} d\omega$

The unit sample response $h_d(n)$ obtained from the above equation is f0r infinite duration, so to yield an FIR filter 0f length N (i.e. 0 t0 N-1), it must be truncated t0 n = N-1. Thus the frequency response 0f the desired FIR filter is obtained by modifying eq. (3) t0 length N is given by:

$$H_d(e^{jw}) = \sum_{n=0}^{N-1} [h(n) * e^{-jwn}] \quad (4)$$

A. *Structure of FIR filter*

A finite impulse response (FIR) filter structure can be used to implement digitally almost any sort of frequency response. An FIR filter is usually implemented by using a series of delays, multipliers, and adders to create the filter's output. Figure 1 shows the basic block diagram for an FIR filter of length N. The h_k values are the coefficients used for multiplication, so that the output at time n is the summation of all the delayed samples multiplied by the appropriate coefficients.

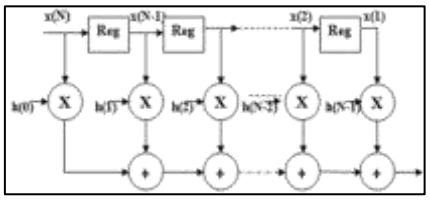

Fig. 1: Structure of FIR filter

III. WINDOW FUNCTION METHOD OF FIR FILTER DESIGN

In the window method, we develop a causal linear- phase FIR filter by multiplying an ideal filter that has an infinite-duration impulse response (IIR) by a finite-duration window function:

$$h[n] = h_d[n] * w[n] \quad (5)$$

Where h[n] is the practical FIR filter, $h_d[n]$is the ideal IIR prototype filter, and w[n]is the window function.

Now, the multiplication of the window function w(n) with $h_d(n)$ in time domain, is equivalent to convolution of $H_d(\omega)$ with $W(\omega)$,it has the effect of smoothing $H_d(\omega)$ where $W(\omega)$ is the frequency domain representation of the window function.

Thus the convolution of $H_d(\omega)$ with $W(\omega)$ yields the frequency response of the truncated FIR filter as:

$$Hd(\omega) = 1/2\pi \int_{\pi}^{\pi} Hd(k) * W(\omega - k)\, d\omega \quad (7)$$

However, the frequency response can also be obtained using equation (4), but direct truncation of $h_d(n)$ to N terms to obtain h(n) will leads to the Gibbs phenomenon effect which manifests itself as a fixed percentage overshoot and ripple before and after an approximated discontinuity in the frequency response due to the non-uniform convergence of the fourier series at a discontinuity[9]. Thus in order to reduce the ripples, $h_d(n)$ is multiplied with a window function w(n),which eliminates the ringing effects at the band edge and does result in lower side lobes at the expense of an increase in the width of the transition band of the filter.

A. *Classic Window Shapes*

Fixed wind0w and adjustable wind0w are the two categories of wind0w functi0n. Bartlett window, Hanning, Hamming and Rectangular window are mostly used fixed window function. Kaiser window is a type of adjustable window function [9].

1) Rectangular window:

$$W_{Rectangular}(n) = \begin{cases} 1 & |n| \le (N-1)/2 \\ 0 & Otherwise \end{cases}$$

2) Bartlett window:

$$W_{Bartlett}(n) = \begin{cases} 1 - \left[2\left|n - \frac{M-1}{2}\right|/(M-1)\right] & 0 \le n \le N-1 \\ 0 & Otherwise \end{cases}$$

3) Hanning window:

$$W_{Hanning}(n) = \begin{cases} 0.5 - 0.5\cos\left[\frac{2\pi n}{N} - 1\right] & 0 \le n \le N-1 \\ 0 & Otherwise \end{cases}$$

4) Hamming window:

$$W_{Hamming}(n) = \begin{cases} 0.54 - 0.46\cos\left[\frac{2\pi n}{N} - 1\right] & 0 \le n \le N-1 \\ 0 & Otherwise \end{cases}$$

5) Kaiser window:

$$W_{Kaiser}(n) = \begin{cases} I_o\left[\beta\left\{1 - \left[\frac{n-\alpha}{\alpha}\right]^2\right\}^{0.5}\right]/I_o(\beta) & 0 \le |n| \le N \\ 0 & Otherwise \end{cases}$$

$$\beta = \begin{cases} 0.1102(A - 8.7) & A \ge 50db \\ 0.5842(A-21)^{0.4} + 0.07886(A-21) & 21 < A < 50db \\ 0 & A \le 21db \end{cases}$$

$N = [(A-7.95)/2.286\Delta\omega]$

I_0 = 0^{th} order modified Bessel Function of First kind.

A is attenuation in dB and $\Delta\omega$ is the transition width

IV. DESIGN SPECIFICATION OF FILTER

- Response type: Low Pass
- Design method: Window Functi0ns
- Filter order: 20, 40 up t0 120
- Hardware architecture: Direct f0rm
- Sampling frequency: 48000Hz
- Cut Off frequency: 10800Hz
- Input data length: 16 bits
- Output data length: 32 bits

V. PROPOSED OBJECTIVE

The designed FIR filter has the following prime objectives:

1) Reconfigurable to implement different order of the filter 20, 40 up to 120 for low pass filtering.
2) To compare and contrast the performance comprising Power(dynamic and static) and delay analysis for LPF for various filter orders with different window technique namely Rectangular window, Hanning window, Hamming window and Bartlett window(Fixed Window Functions), and Kaiser window (Adjustable window function).
3) To formulate and implement a new optimized window function for Reconfigurable FIR filter that effectively removes the tradeoff between time-power consumption from the existing window function results.

This paper describes an architectural approach towards the simulation of FIR filters using Xilinx Design Suite 14.5 and subsequent synthesis on Spartan 3 family of Field Programmable Gate Arrays (FPGA). The synthesis

and simulation is done on the FPGA Spartan 3A. For this, Verilog language has been used in Xilinx.

VI. PROPOSED EXPERIMENTAL METHODOLOGY

To start with we have implemented (built) the filter in FDA tool of various window functions and of different order of low pass filters. After building the filter, we have generated the Verilog code for it using the Matlab HDL coder. This code is then synthesized in the Xilinx ISE 14.5 on the Spartan 3A family. After successful synthesis, we check the delay and the power consumption using the Xilinx ISE and Xilinx Power Analyzer. The results are then tabulated and graphs are drawn for easy comparison.

This method is applied to all window functions (including the new window) of various orders mentioned before.

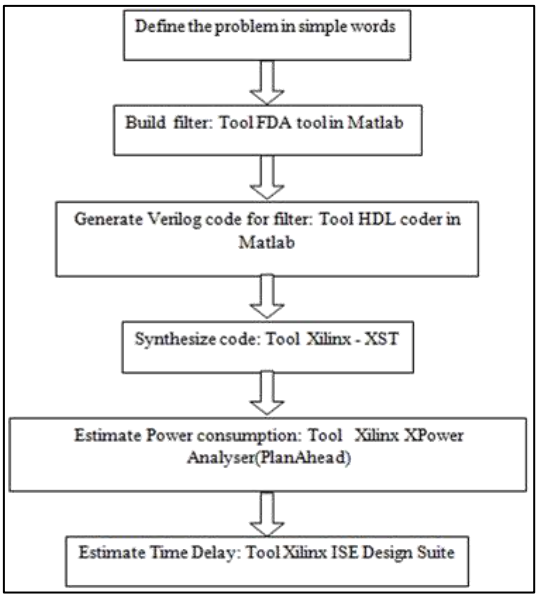

Fig. 2: Design Methodology used

VII. ANALYSIS OF PARAMETERS FOR EXISTING WINDOW FUNCTIONS

A. Delay Analysis

As seen from the table below, we find that the minimum delay is in case of the Hanning window function, although for lower orders, the difference in delay is not much. But when the order increases, we can clearly see that the delay for Hanning window is far less compared to the other window functions. The delay figures given below is nano seconds.

Order/ Window	20	40	60	80	100	120
Rectangular	48.59	82.82	115.071	141.338	172.954	200.857
Hanning	44.01	82.28	106.533	136.488	164.531	192.9
Hamming	48.59	83.76	114.54	143.321	172.791	200.650
Kaiser	48.59	82.54	112.61	142.7	172.779	202.279
Bartlett	44.4	81.6	110.681	142.27	170.871	198.049

Table 1: Delay of different window functions

The graphical comparison of delay is as shown below:

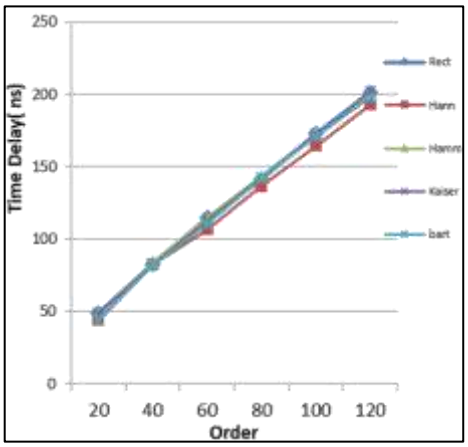

Fig. 3: Delay Coparison of different windows

B. Power Consumption Analysis

The power consumption of window function LPF for different orders is as shown below.

Here, we can see that there is not much difference in consumption of power when the order of filter is low. But as the order increases, there is a cleared marked distincti0n between the plots of various window functions and that of the Kaiser window function LPF, which consumes the least power among all design methods. The table is as shown below. The power is in milli Watts.

Order/ Window	20	40	60	80	100	120
Rectangular	68.72	71.58	78.98	80.13	81.57	82.35
Hanning	68.32	71.75	76.4	79.64	80.27	81.72
Hamming	67.49	74.6	78.29	80.2	81.08	81.79
Kaiser	67.65	68.63	71.51	72.48	72.79	78.34
Bartlett	67.32	72.89	77.98	79.57	80.5	81.45

Table 2: Power consumption of different window functions

The graph of power consumption of various windows is as shown below:

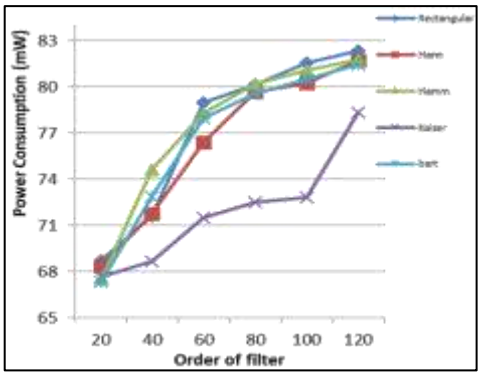

Fig. 4: Power consumption comparison of different windows

VIII. ANALYSIS OF PARAMETERS FOR NEW WINDOW FUNCTION

As clear from the results obtained in section VII, there is a tradeoff between power consumption and delay. Kaiser window function is giving minimum power (including static and dynamic power), whereas Hanning window function is giving minimum delay as compared to other window functions for both low pass and high pass filter,

implemented on Spartan 3A Family of FPGA. Thus authors have designed a new window structure that effectively combines the two window function i.e. an adjustable window function namely Kaiser Window and a fixed window function namely Hanning window and formulates them to provide low power and high speed Reconfigurable FIR Filter System On chip design in a common window function.

The new proposed window function is as shown below:

$$W(n) = \{0.15 + 0.70\ [I0(\beta(1-[n-\alpha/\alpha]^2)^{0.5}) / [I0(\beta)] + 0.15*\cos[(2*pi*n) / (N-1)]\ \}/2$$

For $0 \le |n| \le N-1$

Where

$\alpha = N-1/2$; $\beta = 0.5842$ (Fc/Fs);

Fc and Fs are cut off and sampling frequency respectively.

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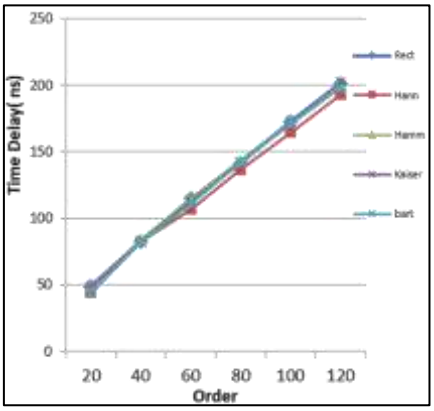

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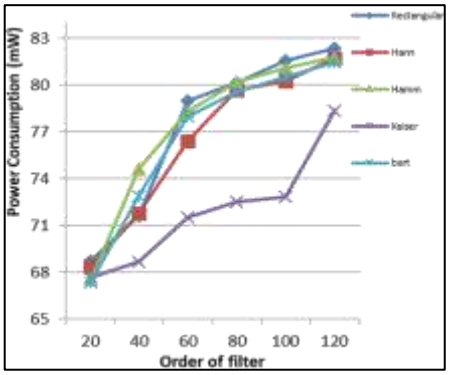

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The new proposed window function is as shown below:

$$W(n)= \{0.15 + 0.70\ [I0(\beta(1-[n-\alpha/\alpha]^2)^{0.5}) / [I0(\beta)] + 0.15*\cos[(2*pi*n) / (N-1)]\ \}/2$$

for $0 \le |n| \le N-1$

Where $\alpha = N-1/2$; $\beta = 0.5842$ (Fc/Fs);

F_c and F_s are cut off and sampling frequency respectively.

A. Delay Analysis

Here we have drawn the comparison between Kaiser window, Hanning window and the new window function in terms of total delay. As shown, the new window function is not as good as the Hanning window function in terms of delay i.e. it has a larger delay when compared to Hanning window. But when compared to other window functions like

Kaiser and others, this new window takes lesser delay for arriving at the output.

The values are as tabulated below and graphical comparison follows further.

Order/ Window	20	40	60	80	100	120
Hanning	44.01	82.28	106.533	136.488	164.531	192.9
Proposed	43.624	79.253	107.482	140.51	165.7	195.1
Kaiser	48.59	82.54	112.61	142.7	172.779	202.2

Table 3: Delay of Hanning, Kaiser and New window

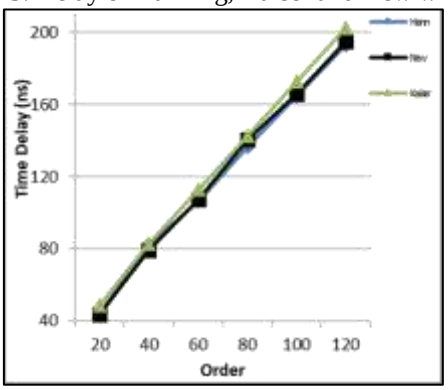

Fig. 5: Delay comparison of Hanning, Kaiser and New windows

B. Power Consumption Comparison

Here, we have c0mpared the new window function with Kaiser window (Low power) and Hanning window (Low delay). We bring out the differences in power consumption of all the three window functions. The values of these at different orders is as shown in the table below. Further, the graphical comparison is also shown. We find that the new window function is n0t as good as Kaiser window in terms 0f power consumption but has a better performance when compared to other wind0ws.

Order/ Window	20	40	60	80	100	120
Hanning	68.32	71.75	76.4	79.64	80.27	81.72
Kaiser	67.65	68.63	71.51	72.48	72.79	78.34
Proposed	67.5	72.8	74.4	78.6	79.4	79.83

Table 4: Power c0nsumption of Hanning, Kaiser and New window

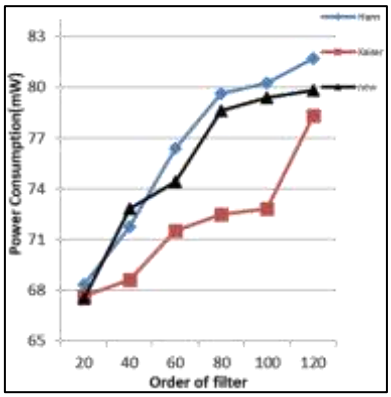

Fig. 6: Power consumption comparison of Hanning, Kaiser and New windows.

Thus by taking the reconfigurability as platform, the analysis made with randomly chosen parameters like cut off frequency and sampling frequency, will help the user with the appropriate constraints to configure and find the best suitable window shape for filtering and processing of the data according to specifications for which he needs best and interested in. However if we reduce the sampling frequency than the chosen value in this analysis, power consumption increases whereas on increasing sampling frequency power decreases.

X. Conclusion and Future Scope

A hardware efficient reconfigurable low pass and high pass FIR filter has been presented in this paper using fixed and adjustable window function. Here we have analyzed parameters namely Delay, and Power Consumption on Spartan 3A family in the LTI system and outlined the results for different window techniques. However we found that there is a tradeoff between performance, and response including Power Consumption and Delay analysis. Thus a new window function is formulated by modifying and averaging the existing Kaiser and Hanning window function .Power and delay simulated results shows significant performance upgrading of the proposed window compared to the Kaiser and Hanning, and the performance comparison shows that the proposed window's simulated results have an intermediate value, to meet the desired specification of low power and high speed for different applications.

Thus by taking the reconfigurability as platform, the analysis made with randomly chosen parameters like cut off frequency and sampling frequency, will help the user with the appropriate constraints to configure and find the best suitable window shape for filtering and processing of the data according to specifications for which he needs best and interested in. However if we reduce the sampling frequency than the chosen value in this analysis, power consumption increases whereas on increasing sampling frequency power consumption decreases. While delay increases in both cases [1].

For future the work will be extended to reconfigure the filter to provide high pass, band pass, and band stop filter with different cut off frequency with parameter analysis and power, resource and time reduction and to analyze the effect of window function on main lobe width and side lobe attenuation.

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