Analysis and Design of Efficient Multipliers by Modified Adders using Various Logic

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Abstract— *Designing an efficient circuit with low power consumption is one of the essential factor for VLSI circuit designers. Many arithmetic operations are performed using multipliers due to its high-speed integration purpose, so to construct an efficient multiplier, adders plays a vital role. Multipliers are the key components in Digital Signal Processors, FIR filter, Microprocessor, graphics, multimedia, etc. To achieve the desired performance a well-planned multiplier can be designed using different logic styles such as pass transistor, 2-T logic and GDI model. The multiplier circuit was designed by using Tanner EDA 180nm technology. The result of proposed method displays an area efficiency of 57.2% and delay efficiency of 13.6% compared to the extant way.*

Keywords— Multiplier, Adder, Pass Transistor, 2-T logic, GDI Cell, Tanner EDA

I. INTRODUCTION

Very Large Scale Integration (VLSI) circuits were designed by fabricating millions of transistors in a single silicon chip. In 1970's the design of VLSI began during that period complex semiconductor and communication technologies were developed. Electronic circuits consist of CPU, RAM, ROM and other elements, but nowadays all these components are integrated with a single chip using VLSI technology. Area, speed, power are three major concern for VLSI designers.

To design a multiplier, there are a lot of constraints like power consumption, transistor count, noise immunity, good driving ability and performance of the circuit. Multipliers are built using binary adders and it is one of the essential functions performed by ALU which requires a faster implementation but, this design occupies a complex area and low-speed process. To eliminate these problems a well-designed technique is to be developed by using various logic styles, it includes pass transistor, 2-T logic, GDI cell. Binary adders are designed using the combinations of AND gate, EXOR gate and OR gate it consists of three inputs and two outputs, that denote sum and carry bits of the block. In this project, the adders [5] are constructed using 2:1 MUX [6] and GDI cell based EXOR gate, by doing this process delay is minimized and efficiency is increased, when the EXOR block in the conventional full adder is replaced by a proposed full adder. This type of adder is used in the construction of multiplier in a well-ordered manner to make it more efficient and usable in various applications.

II. LITERATURE SURVEY

A. Pass Transistor

It is single MOSFET which passes the signal between the drain and source terminals instead of a fixed power supply value. An organised and widely used alternative to complementary CMOS is pass transistor logic [1]which is mainly used to reduce the number of transistors needed to construct the logic by allowing the inputs to drive gate terminals as well as source drain terminals. Two types of pass transistor are available they are

1) N-MOS pass transistor
2) P-MOS pass transistor

N-MOS pass transistors are widely used in much industrial application because N-type material acts as an acceptor.

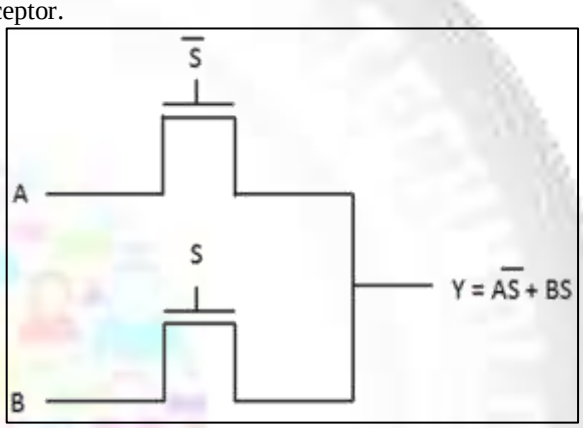

Fig. 1: Pass Transistor Logic

B. 2-T Logic

This logic is mainly used to overcome the drawback in pass transistor logic; this can be done by using CMOS logic which is a combination of both the P-MOS and N-MOS. The extra use of inverter in pass transistor is reduced by using a P-MOS transistor which acts as an inventor to one of the input.

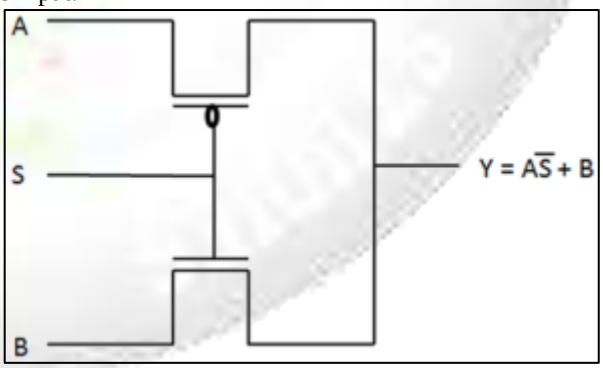

Fig. 2: 2-T logic

C. GDI Cell

The GDI cell is more compact and flexible when compared to static C-MOS gates and have very less leakage current. It consists of only two transistors it appears same as an inverter. GDI cell [9] contains three inputs, P input to source/drain of P-MOS, N input to Source/drain of N-MOS, G input to common gate input to both P-MOS and N-MOS.

The main aim of this technique is to reduce the area and delay.

N	P	G	Out	Function
0	B	A	$\overline{A}B$	F1
B	1	A	$\overline{A}$ + B	F2
1	B	A	A + B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}B$ + AC	MUX
0	1	A	$\overline{A}$	NOT

Table 1: Boolean Function of GDI Cell

1) EXOR Design using GDI Cell:

By using this technique the count of transistor is reduced from 12 transistors to 2 transistors, this is mainly used to increase the efficiency of the EXOR [2] used in the proposed adder design.

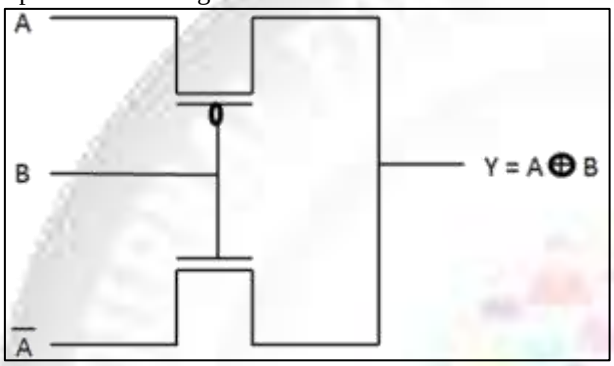

Fig. 3: EXOR using GDI Cell

2) AND GATE using GDI Cell:

Conventional AND gate requires 6 transistors but GDI cell based AND gate requires only 2 transistors. The modified AND gate is used in the construction of multipliers [3] and are used as a partial products in the design.

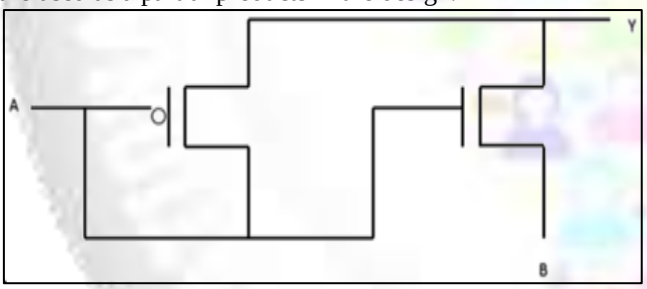

Fig. 4: Modified AND Gate

3) CONVENTIONAL FULL ADDER:

The conventional full adder [7] is very complex because it contains two EXOR gate so that the efficiency is not satisfied in terms of area, power and delay.

$$Sum = A \oplus B \oplus C$$

$$Cout = (A.B) + (C.(A \oplus B))$$

Delay = 2 EXOR

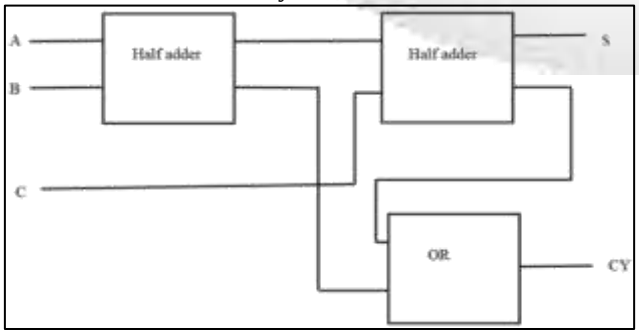

Fig. 5: Conventional Full Adder Design

III. PROPOSED FULL ADDER

The modified full adder circuit consists of two 2:1 MUX and GDI cell based EXOR gate.

Delay = EXOR + MUX

The above expression can be constructed by using second MUX where EXOR output act as a selection line. Mainly EXOR consumes most of the power consumption in adder circuit, by reducing the number of EXOR gates power consumption of the full adders can be reduced. The EXOR gate can also be made efficient by using GDI cell based design. The GDI cell design is mainly constructed to increase the efficiency of the proposed adder design.

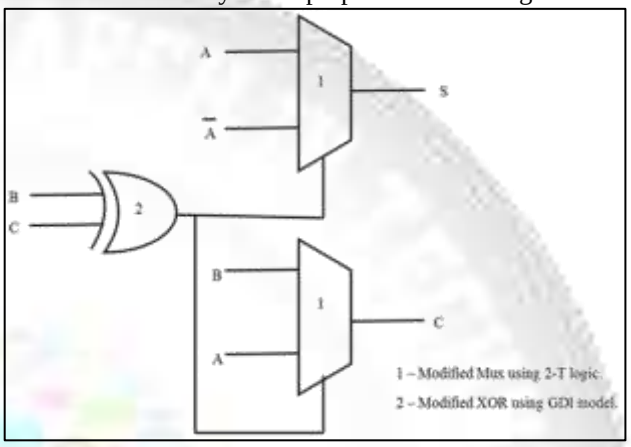

Fig. 6: Modified Full Adder

A. Operation

When both B and C are 0 or 1, Sum = A
When either B or C is 1 and another is 0, Sum = A
When both B and C are 0 or 1, Carry = B
When either B or C is 1 and another is 0, Carry=A
The proposed full adder works with the help of the above operation.

IV. PROPOSED MULTIPLIER DESIGN

After obtaining the logic for the modified 2-T MUX and EXOR using GDI cell the proposed full adder design is constructed. The multiplier block is designed by combining the AND gate and the modified full adder module. The AND gate can be made efficient by using 2 transistors GDI cell technique and it is mainly used to obtain the partial products and the modified MUX based full adder is used, to sum up these products together.

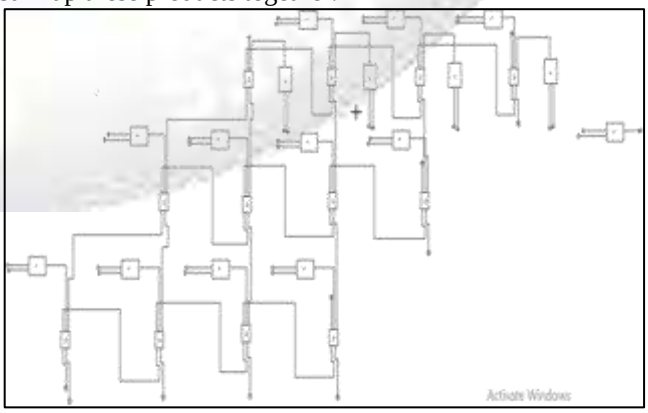

Fig. 7: Proposed Multiplier using MUX Based Adder

The above Fig.7 denotes the 4-bit multiplier circuit. It needs 16 AND gates and 12 full adders, totalling to about 72 MOSFETS are used in the design.

When inputs are given in the following order, the output will be displayed as given in the Fig.8

A0 = 11000111 B0 = 10101111
A1 = 00101001 B1 = 01000011
A2 = 01000101 B2 = 01000000
A3 = 10101001 B3 = 01000100

The following equation denotes the equation for the 4-bit multiplication

A3 A2 A1 A0 * B3 B2 B1 B0 = P7 P6 P5 P4 P3 P2 P1 P0

Where P7, P6, P5, P4, P3, P2, P1, P0 are the outputs of the 4-bit multiplication process.

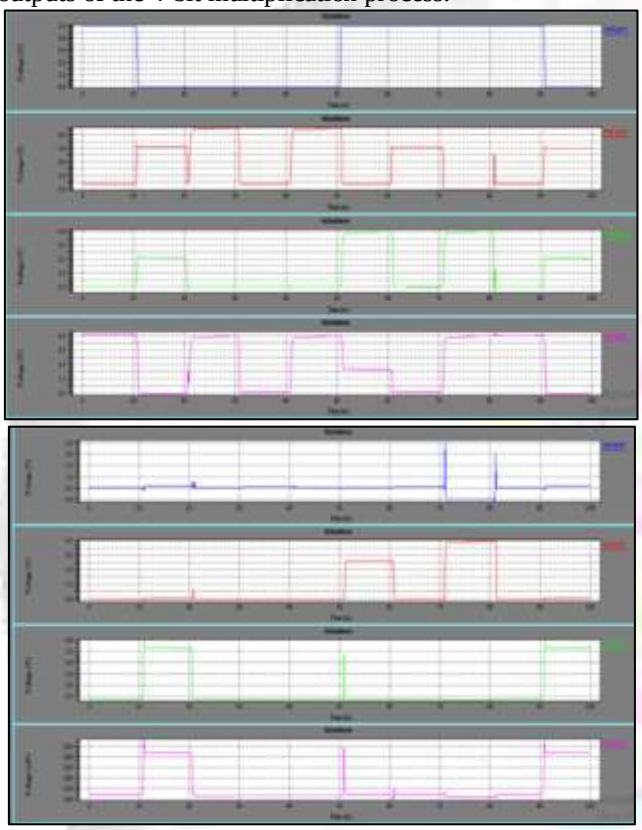

Fig. 8: Output for Proposed Multiplier

V. COMPARISON TABLE

Types of 4-bit Multipliers	Tranistors Used	Delay
Conventional Multiplier	168	10.56n
MUX based Multiplier	168	10.56n
Pass transistor based Multiplier	88	9.40n
2-T Logic based Multiplier	72	9.12n

Table 2: Various Multipliers Comparison Table

The above table is used to compare the multiplier designs that have been implemented using various logics. The parameters such as the number of transistors and delay have been analysed.

A. Analysis Graph

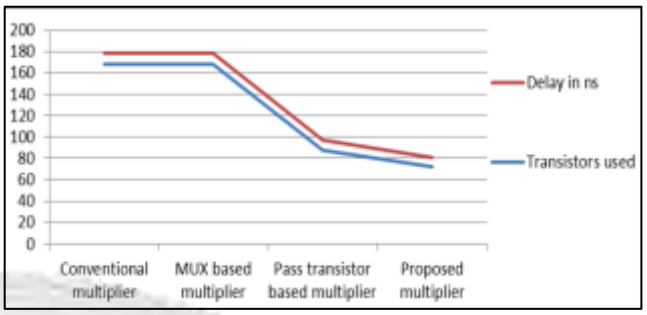

Fig. 9: Analysis of Various Logic Multipliers

B. Applications

Multipliers are widely used in the arithmetic operation in many applications they are listed below.

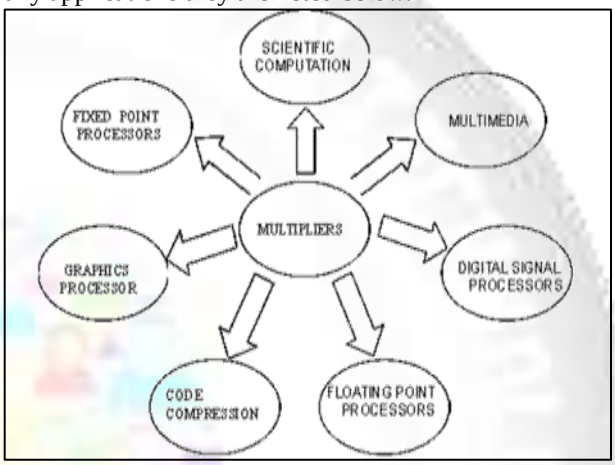

Fig. 10: Applications of Multipliers

VI. CONCLUSION

In this paper we have designed an efficient and a fast multiplier, the logic is proposed as a suitable design that involves few transistor with low power consumption that includes the switching power, short circuit power, and static power. This process of designing will not only increase the speed of the circuit but work presented in this project will achieve good results and also the demonstration of high-level optimization techniques.

A. Future Enhancements

The multiplier design proposed in our project will provide a considerable level of improvement over various parameters. In the future, we will focus on various other logic designs such as multipliers, FIR filters and other higher-end circuits that will give a further development over various parameters and hence it results in higher level of efficiency.

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